

**3N204, 3N205, 3N206****Silicon Dual Insulated-Gate  
Field-Effect Transistors**

With Integrated Gate-Protection Circuits for VHF TV  
Applications

3N204 — RF Amplifier 3N205 — Mixer  
3N206 — TV IF Amplifier

**Features:**

- Low  $C_{rss}$  — 0.03 pF max.
- High  $|Y_{fs}|$  — 14 mmho typ. for 3N204 and 3N205
- Integrated gate-protection diodes

The RCA-3N204, 3N205, and 3N206 are n-channel silicon, depletion type, dual-insulated gate, field-effect transistors intended for vhf TV applications. Integrated back-to-back diodes protect the gates from excessive input voltages.

The 3N204 is intended for use in vhf rf amplifiers and delivers linear, low-noise amplification. Its extremely low feedback

capacitance allows high-gain stable operation without neutralization. The 3N205 is specified for low noise vhf mixer applications. The 3N206 is intended for use in tuned high-frequency amplifiers such as TV if strips.

**Maximum Ratings, Absolute-Maximum Values at  $T_A = 25^\circ$ :**

* DRAIN-TO-GATE No. 1 VOLTAGE .....	30 V
* DRAIN-TO-GATE No. 2 VOLTAGE .....	30 V
* DRAIN-TO-SOURCE VOLTAGE .....	25 V
* GATE No.1-TERMINAL FORWARD CURRENT <sup>▲</sup> .....	10 mA
* GATE No.2-TERMINAL FORWARD CURRENT <sup>▲</sup> .....	10 mA
* GATE No.1-TERMINAL REVERSE CURRENT .....	-10 mA
* GATE No.2-TERMINAL REVERSE CURRENT .....	-10 mA
* CONTINUOUS DRAIN CURRENT .....	50 mA
* DEVICE DISSIPATION:	
Up to $T_A = 25^\circ\text{C}$ .....	360 mW
Above $T_A = 25^\circ\text{C}$ derate linearly .....	2.4 mW/ $^\circ\text{C}$
Up to $T_C = 25^\circ\text{C}$ .....	1.2 W
Above $T_C = 25^\circ\text{C}$ derate linearly .....	8 mW/ $^\circ\text{C}$
* AMBIENT TEMPERATURE RANGE:	
Operating .....	-65 to +175 $^\circ\text{C}$
Storage .....	-65 to +200 $^\circ\text{C}$
* LEAD TEMPERATURE (During Soldering):	
At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79$ mm) from case for 10 seconds max. ....	+300 $^\circ\text{C}$

- <sup>▲</sup> Forward gate-terminal current is the current into a gate terminal with a forward-gate-to-source voltage applied. This voltage is of such polarity that an increase in its magnitude causes the channel resistance to decrease.
- \* In accordance with JEDEC registration data format (JS-9 RDF-19B).

## 3N204, 3N205, 3N206

ELECTRICAL CHARACTERISTICS, At  $T_A = 25^\circ\text{C}$  (unless otherwise specified)

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS	
		MIN.	MAX.		
* Drain-to-Source Breakdown Voltage, $V_{(BR)DS}$	$I_D = 10\mu\text{A}$ , $V_{G1S} = V_{G2S} = -5\text{V}$	25	-	V	
* Gate No.1-to-Source Forward Breakdown Voltage, $V_{(BR)G1SSF1}$	$I_{G1} = 10\text{mA}$ , $V_{G2S} = V_{DS} = 0$	6	30	V	
* Gate No.1-to-Source Reverse Breakdown Voltage, $V_{(BR)G1SSR1}$	$I_{G1} = -10\text{mA}$ , $V_{G2S} = V_{DS} = 0$	-6	-30	V	
* Gate No.2-to-Source Forward Breakdown Voltage, $V_{(BR)G2SSF1}$	$I_{G2} = 10\text{mA}$ , $V_{G1S} = V_{DS} = 0$	6	30	V	
* Gate No.2-to-Source Reverse Breakdown Voltage, $V_{(BR)G2SSR1}$	$I_{G2} = -10\text{mA}$ , $V_{G1S} = V_{DS} = 0$	-6	-30	V	
* Gate No.1-Terminal Forward Current, $I_{G1SSF}$	$V_{G1S} = 5\text{V}$ , $V_{G2S} = V_{DS} = 0$	-	10	nA	
* Gate No.1-Terminal Reverse Current, $I_{G1SSR}$	$V_{G1S} = -5\text{V}$ , $V_{G2S} = V_{DS} = 0$	$T_A = 25^\circ\text{C}$	-	-10	nA
		$T_A = 150^\circ\text{C}$	-	-10	$\mu\text{A}$
* Gate No.2-Terminal Forward Current, $I_{G2SSF}$	$V_{G2S} = 5\text{V}$ , $V_{G1S} = V_{DS} = 0$	-	10	nA	
* Gate No.2-Terminal Reverse Current, $I_{G2SSR}$	$V_{G2S} = -5\text{V}$ , $V_{G1S} = V_{DS} = 0$	$T_A = 25^\circ\text{C}$	-	-10	nA
		$T_A = 150^\circ\text{C}$	-	-10	$\mu\text{A}$
* Zero-Gate No.1-Voltage Drain Current, $I_{DS}^2$	$V_{DS} = 15\text{V}$ , $V_{G1S} = 0$ , $V_{G2S} = 4\text{V}$	3N204	6	30	mA
		3N205	6	30	
		3N206	3	15	
* Gate No.1-to-Source Cutoff Voltage, $V_{G1S(\text{off})}$	$V_{DS} = 15\text{V}$ , $V_{G2S} = 4\text{V}$ , $I_D = 20\mu\text{A}$	-0.5	-4	V	
* Gate No.2-to-Source Cutoff Voltage, $V_{G2S(\text{off})}$	$V_{DS} = 15\text{V}$ , $V_{G1S} = 0$ , $I_D = 20\mu\text{A}$	-0.2	-4	V	
* Small-Signal Common-Source Forward Transfer Admittance, $ y_{fs} ^3$	$V_{DS} = 15\text{V}$ , $V_{G1S} = 0$ , $V_{G2S} = 4\text{V}$ , $f = 1\text{ kHz}$	3N204	10	22	mmho
		3N205	10	22	
		3N206	7	17	
* Small-Signal Common-Source Reverse Transfer Capacitance, $C_{rss}$	$V_{DS} = 15\text{V}$ , $V_{G2S} = 4\text{V}$ , $I_D = 10\text{ mA}$ , $f = 1\text{ MHz}$	0.005	0.03	pF	

\*In accordance with JEDEC registration data format (JS-9 RDF-19B).

- All gate breakdown voltages are measured while the device is conducting rated gate current. This ensures that the gate-voltage-limiting network is functioning properly.
- This characteristic must be measured using pulse techniques ( $t_W = 300\mu\text{s}$ , duty cycle  $\leq 2\%$ ).
- This characteristic must be measured with bias voltages applied for less than 5 seconds to avoid overheating. The signal is applied to gate No.1 with gate No.2 at ac ground.

Small-Signal MOSFETs

3N204, 3N205, 3N206

OPERATING CHARACTERISTICS at  $T_A = 25^\circ\text{C}$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
<b>3N204</b>					
* Common-Source Spot Noise Figure, NF		-	-	3.5	dB
* Small-Signal Common-Source Insertion Power Gain, $G_{ps}$	$V_{DD}=18\text{ V}, V_{GG}=7\text{ V}, f=200\text{ MHz}, \text{ See Fig. 13}$	20	-	28	dB
* Bandwidth, BW		7	-	12	MHz
* Gain-Control Gate-Supply Voltage, $V_{GG}(\text{GC})$	$V_{DD}=18\text{ V}, \Delta G_{ps}=-30\text{ dB}, f=200\text{ MHz}, \text{ See Fig. 13}$	0	-	-2	V
* Common-Source Spot Noise Figure, NF	$V_D=15\text{ V}, V_{G2S}=4\text{ V}, f=450\text{ MHz}, I_D=10\text{ mA}, \text{ See Figs. 15 and 16}$	-	-	5	dB
* Small-Signal Common Source Insertion Power Gain, $G_{ps}$		14	-	-	dB
<b>3N205</b>					
* Small-Signal Conversion Power Gain, $G_{ps}(\text{conv})$	$V_{DD}=18\text{ V}, f_{LO}=245\text{ MHz}, f_{RF}=200\text{ MHz}, \text{ See Fig. 17}$	17	-	28	dB
* Bandwidth, BW		4	-	7	MHz
<b>3N206</b>					
* Common-Source Spot Noise Figure, NF		-	-	4	dB
* Small-Signal Common-Source Insertion Power Gain, $G_{ps}$	$V_{DD}=24\text{ V}, V_{GG}=6\text{ V}, f=45\text{ MHz}, \text{ See Fig. 14}$	25	-	35	dB
* Bandwidth, BW		3	-	6	MHz
* Gain-Control Gate-Supply Voltage, $V_{GG}(\text{GC})$	$V_{DD}=24\text{ V}, \Delta G_{ps}=-30\text{ dB}, f=45\text{ MHz}, \text{ See Fig. 14}$	-1.6	-	0.6	V

- \*In accordance with JEDEC registration data format (JS-9 RDF-19B).  
 1.  $\Delta G_{ps}$  is defined as the change in  $G_{ps}$  from the value at  $V_{GG} = 7\text{ V}$ .  
 2.  $\Delta G_{ps}$  is defined as the change in  $G_{ps}$  from the value at  $V_{GG} = 6\text{ V}$ .  
 3. Amplitude at input from local oscillator is 3 V RMS.

TYPICAL CHARACTERISTICS

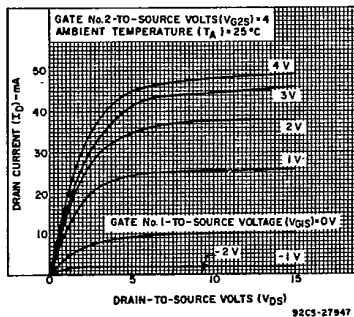


Fig. 1 - Drain current vs. drain-to-source volts (pulse-tested with pulse duration = 300  $\mu\text{s}$ , duty cycle  $\leq 2\%$ ).

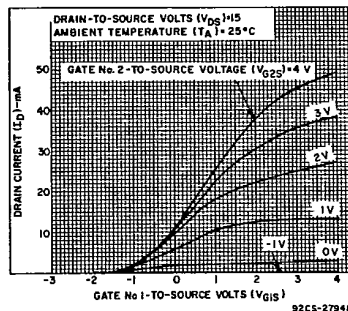


Fig. 2 - Drain current vs. gate-No. 1-to-source volts (pulse-tested with pulse duration = 300  $\mu\text{s}$ , duty cycle  $\leq 2\%$ ).

# 3N204, 3N205, 3N206

## TYPICAL Y-PARAMETER CHARACTERISTICS

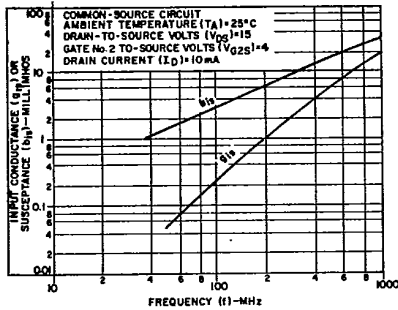


Fig. 3 -  $Y_{fs}$  vs.  $f$

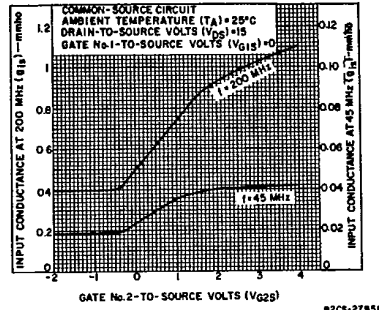


Fig. 4 -  $Y_{fs}$  vs.  $V_{G2S}$

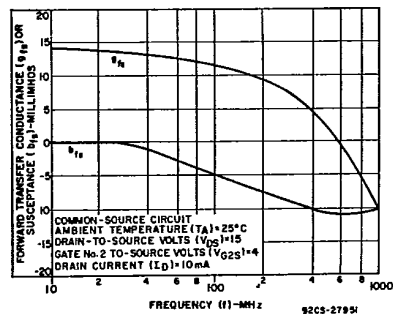


Fig. 5 -  $Y_{fs}$  vs.  $f$

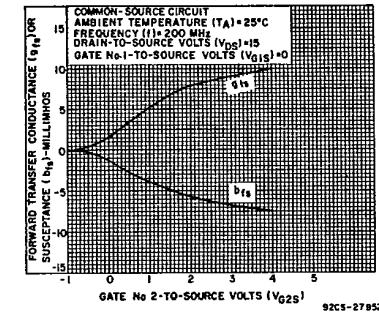


Fig. 6 -  $Y_{fs}$  vs.  $V_{G2S}$

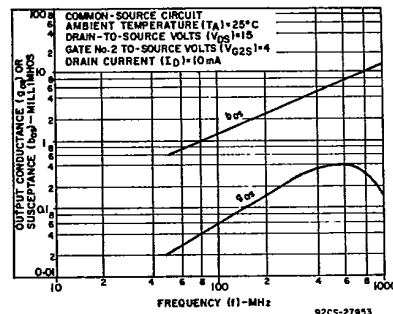


Fig. 7 -  $Y_{os}$  vs.  $f$

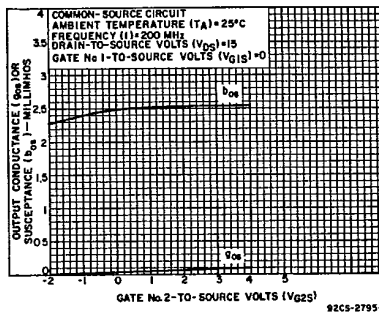


Fig. 8 -  $Y_{os}$  vs.  $V_{G2S}$

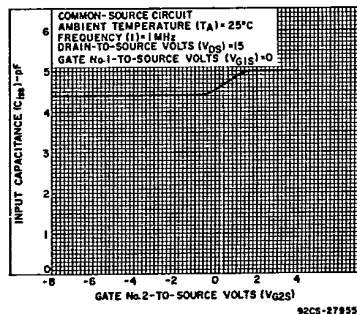


Fig. 9 -  $C_{iss}$  vs.  $V_{G2S}$

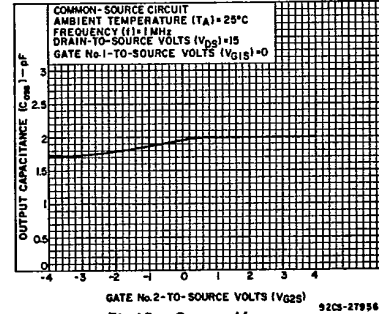


Fig. 10 -  $C_{oss}$  vs.  $V_{G2S}$

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TYPICAL OPERATING CHARACTERISTICS FOR 3N204

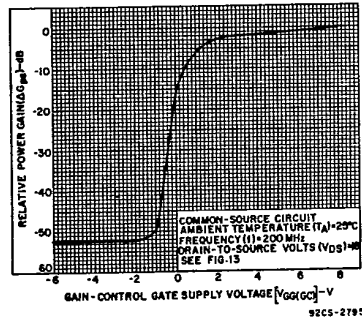


Fig. 11 -  $\Delta G_{ps}$  vs.  $V_{GG}(GC)$

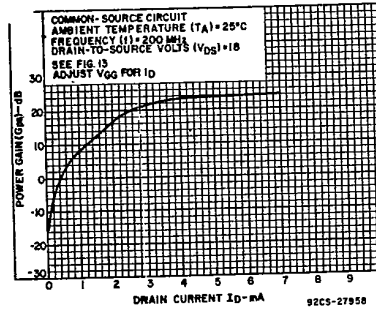
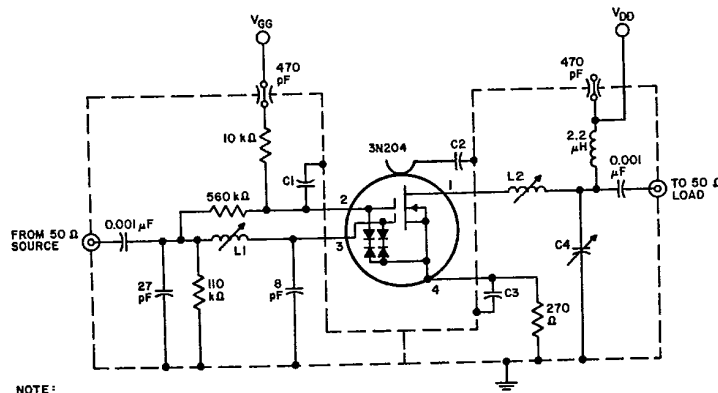


Fig. 12 -  $G_{ps}$  vs.  $I_D$

TEST CIRCUITS



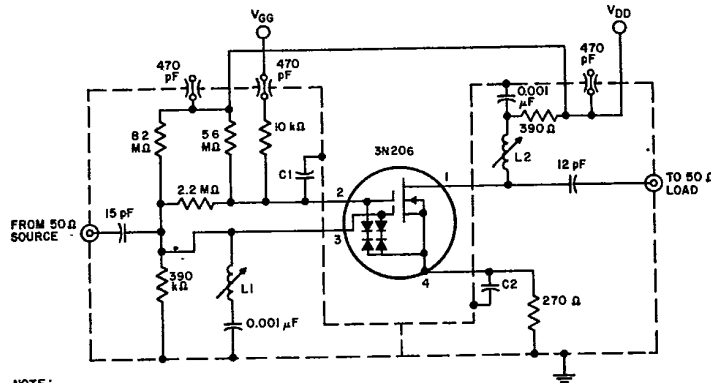
NOTE:  
 C1, C2, & C3: LEADLESS DISC CERAMIC, 0.001 μF  
 C4: ARCO 462, 5-80 pF, OR EQUIVALENT  
 L1: 3 TURNS No. 18 WIRE, 3/16 INCH-DIA ALUMINUM SLUG  
 L2: 9 TURNS No. 20 WIRE, 3/16 INCH-DIA. ALUMINUM SLUG

92CS-27950

Fig. 13 - 200-MHz power gain, gain-control voltage, and noise-figure test circuit for 3N204\*.

\* In accordance with JEDEC registration data format (JS-9 RDF-19B).

3N204, 3N205, 3N206

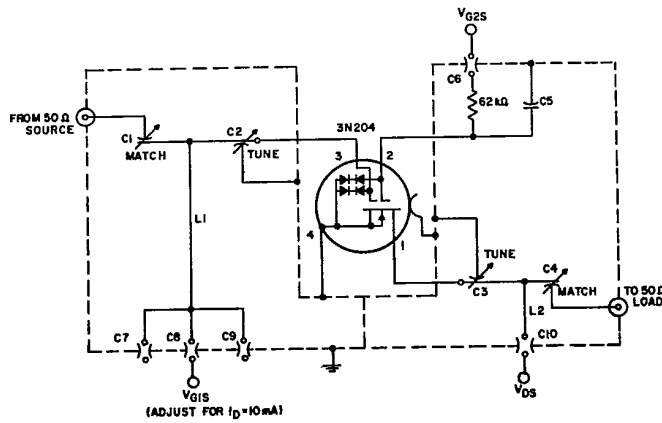


NOTE:  
 C1: LEADLESS DISC CERAMIC, 0.001 μF  
 C2: LEADLESS DISC CERAMIC, 0.01 μF  
 L1: 8 TURNS No. 28 WIRE, 5/32 INCH-DIA. FORM, TYPE "J" SLUG  
 L2: 9 TURNS No. 28 WIRE, 5/32 INCH-DIA. FORM, TYPE "J" SLUG

92CM-27959

Fig. 14 -- -45-MHz power-gain and noise-figure test circuit for 3N206\*.

\* In accordance with JEDEC registration data format (JS-9 RDF-19B).



NOTE:  
 FOR TEST FIXTURE, SEE PICTORAL DRAWING IN FIGURE 16  
 C1 THRU C4: SEE FIGURE 16, NOTE D  
 C5: 0.001 μF LEADLESS DISC CAPACITOR  
 C6 THRU C10: ALLEN-BRADLEY F5AU 0.001 μF FEED-THROUGH CAPACITORS, OR EQUIVALENT  
 L1 & L2: SEE FIGURE 16

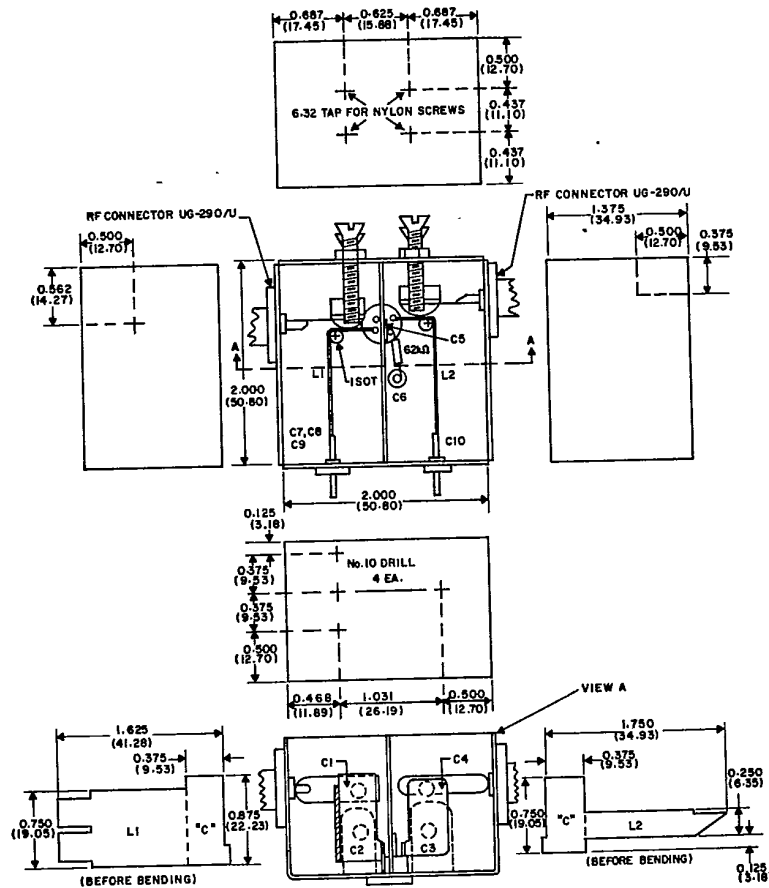
92CM-27961

Fig. 15 -- -450-MHz power-gain and noise-figure test circuit for 3N204\*.

\* In accordance with JEDEC registration data format (JS-9 RDF-19B).

## Small-Signal MOSFETs

## 3N204, 3N205, 3N206



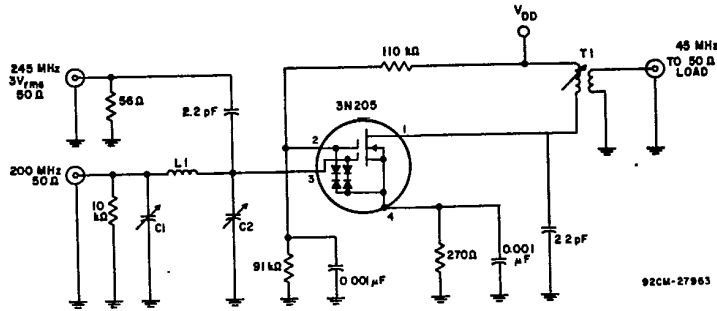
92CL-27962

## NOTES:

- A. Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions, as indicated.
- B. The removable top of test fixture is not shown.
- C. For clarity, the 62 kΩ resistor, the source and gate-2 socket pins, and insulating stand-off terminals (ISOT) soldered into the fold of L1 and L2 respectively for mechanical support, are not shown in view A.
- D. C1 and C2 (C3 and C4) consist of shim brass and the "C" portion of L1 (L2) separated by air and the mylar tape covering the "C" portion of L1 (L2).
- E. The four views surrounding the center view are as they would appear before the metal is bent up to form the sides.

Fig. 16 -- 450 MHz power-gain and noise-figure test fixture\*.

\* In accordance with JEDEC registration data format (JS-9 RDF-19B).



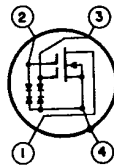
NOTE:  
 C1: ARCO 462, 5-80 pF, OR EQUIVALENT  
 C2: ARCO 460, 1.5-15 pF, OR EQUIVALENT  
 L1: 4 TURNS No.14 WIRE, 1/4 INCH INSIDE DIA.

T1: PRI: 16 TURNS No.30 WIRE CLOSE WOUND  
 ON 1/4 INCH DIA. FORM, TYPE "J" SLUG  
 SEC: 6 TURNS No.30 WIRE CENTERED  
 OVER PRIMARY

Fig.17 -- 200 MHz-to-45-MHz circuit for conversion power gain for 3N205\*.

\* In accordance with JEDEC registration data format (JS-9 RDF-19B).

**TERMINAL DIAGRAM**  
 Bottom View



LEAD 1 - DRAIN  
 LEAD 2 - GATE No.2  
 LEAD 3 - GATE No.1  
 LEAD 4 - SOURCE,  
 SUBSTRATE AND CASE

**OPERATING CONSIDERATIONS**

The flexible leads of these devices are usually soldered to the circuit elements. As is the case with any high-frequency semiconductor device, the tips of soldering irons MUST be grounded.