NEC

SILICON TRANSISTOR
2SD1164-Z

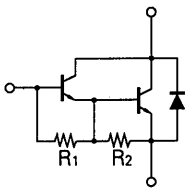
NPN SILICON EPITAXIAL TRANSISTOR
MP-3

DESCRIPTION

2SD1164-Z is designed for Low Frequency Amplifier and Switching, especially in Hybrid Integrated Circuits.

FEATURES

- High h_{FE} = 2 000 to 30 000



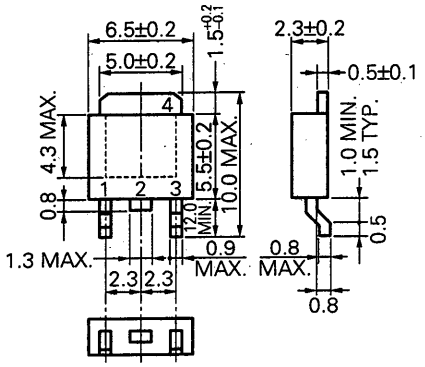
$R_1 \fallingdotseq 10\ k\Omega$
$R_2 \fallingdotseq 500\ k\Omega$

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

PACKAGE DIMENSIONS
(in millimeters)



1. Base
2. Collector
3. Emitter
4. Collector

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Collector to Base Voltage	V_{CBO}	150	V
Collector to Emitter Voltage	V_{CEO}	60	V
Emitter to Base Voltage	V_{EBO}	8.0	V
Collector Current (DC)	I_C	2	A
Collector Current (Pulse)*	I_C	4	A
Total Power Dissipation (T_a = 25 °C)**	P_T	2.0	W
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* PW ≦ 10 ms, Duty Cycle ≦ 50 %

**When mounted on ceramic substrate of 7.5 cm^2 × 0.7 mm

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ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Collector Cutoff Current	I_{CBO}			10	μA	V_{CB} = 60 V, I_E = 0
Emitter Cutoff Current	I_{EBO}			1.0	mA	V_{EB} = 5.0 V, I_C = 0
DC Current Gain	h_{FE1}*	1 000				V_{CE} = 2.0 V, I_C = 0.5 A
DC Current Gain	h_{FE2}*	2 000		30 000		V_{CE} = 2.0 V, I_C = 1.0 A
Collector Saturation Voltage	$V_{CE(sat)}$*			1.5	V	I_C = 1.0 A, I_B = 1.0 mA
Base Saturation Voltage	$V_{BE(sat)}$*			2.0	V	I_C = 1.0 A, I_B = 1.0 mA
Turn-on Time	t_{on}		0.5		μs	I_C = 1.0 A, I_{B1} = $-I_{B2}$ = 1.0 mA V_{CC} ≒ 50 V, R_L = 50 Ω
Storage Time	t_{stg}		1.0		μs	
Fall Time	t_f		1.0		μs	

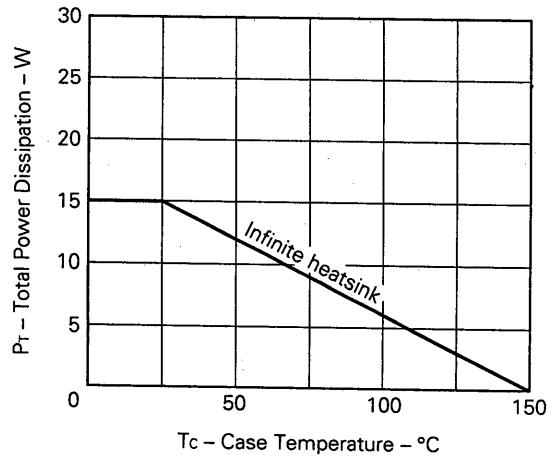
*Pulsed: PW ≦ 350 μs, Duty Cycle ≦ 2 %

h_{FE} Classification

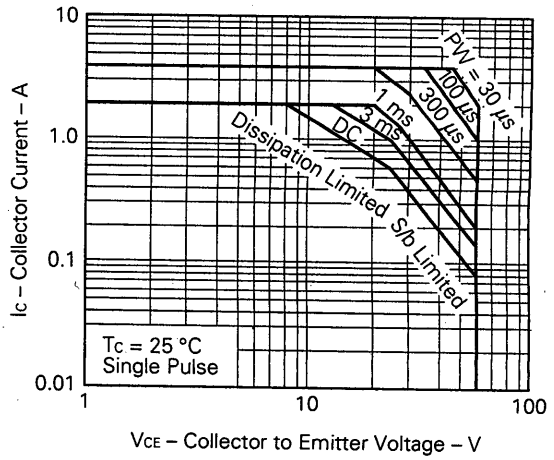
MARKING	M	L	K
h_{FE2}	2 000 to 5 000	4 000 to 10 000	8 000 to 30 000

TYPICAL CHARACTERISTICS (T_a = 25 °C)

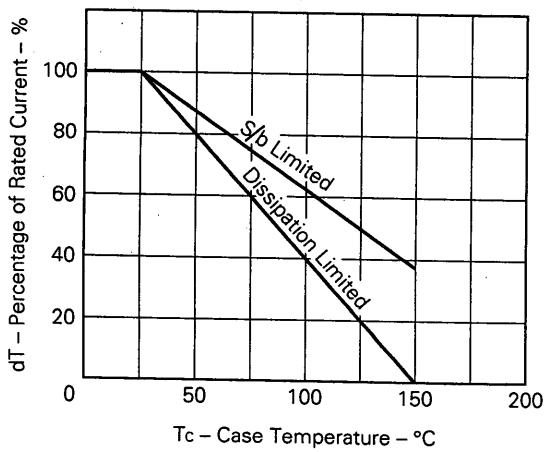
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



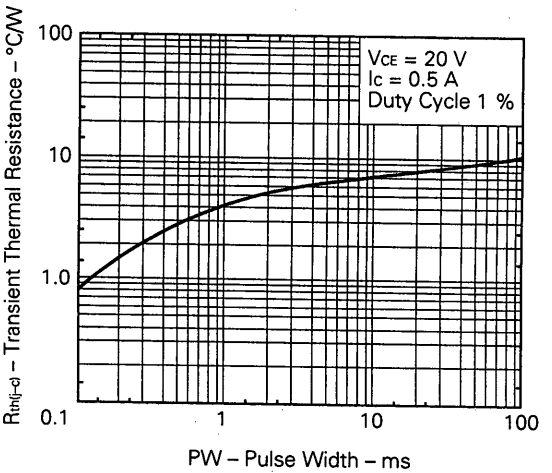
SAFE OPERATING AREA



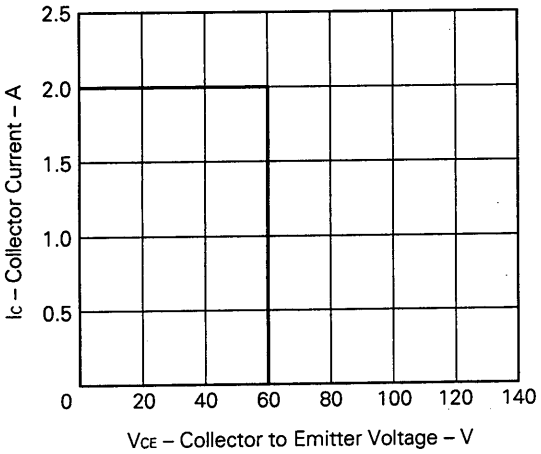
DERATING CURVE OF SAFE OPERATING AREA



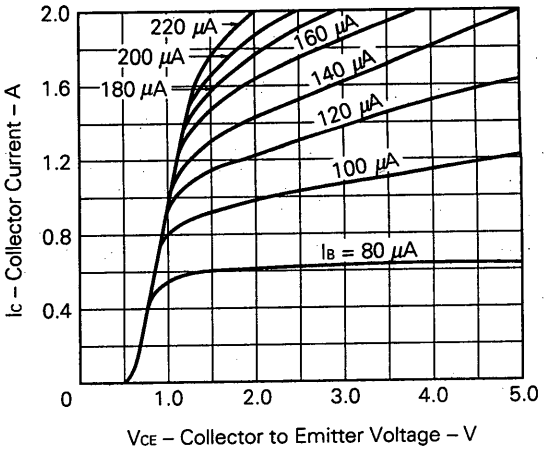
TRANSIENT THERMAL RESISTANCE



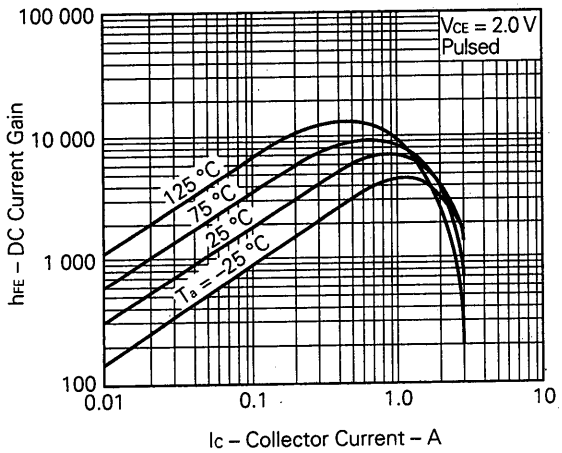
REVERSE BIAS SAFE OPERATING AREA



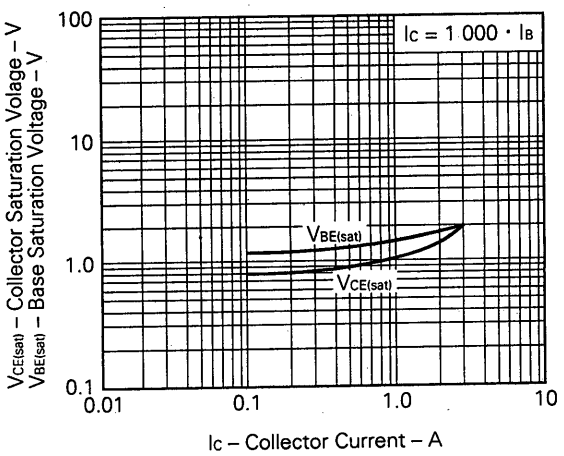
COLLECTOR CURRENT vs.
COLLECTOR TO EMITTER VOLTAGE



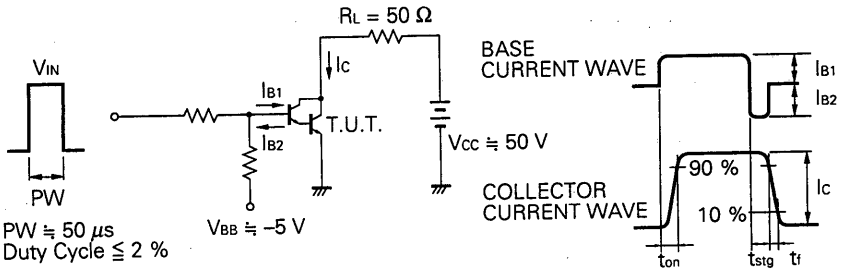
DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION
VOLTAGE vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT



Reference

Application note name	No.
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207
Design of Push-Pull Type Switching Regulators (Basic)	TEB-1002
Design oif Push-Pull Type Switching Regulators (Applications)	TEB-1003
Optimum Base Drive Conditions of Switching Power Transistors	TEB-1014

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