

### FEATURES

- Low  $V_{OS}$  ..... 100 $\mu$ V Max
- Offset Voltage Match ..... 90 $\mu$ V Max
- Offset Voltage Match vs. Temp. .... 1.0 $\mu$ V/ $^{\circ}$ C Max
- Common-Mode Rejection Match ..... 103dB Min
- Bias Current Match ..... 3.5nA Max
- Low Noise ..... 0.6 $\mu$ V<sub>p-p</sub> Max
- Low Bias Current ..... 3.0nA Max
- High Channel Separation ..... 126dB Min

### ORDERING INFORMATION†

$T_A = 25^{\circ}$ C $V_{OS}$ MAX ( $\mu$ V)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
100	OP207AY*	MIL
100	OP207EY	COM
200	OP207FY	COM

\* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

### GENERAL DESCRIPTION

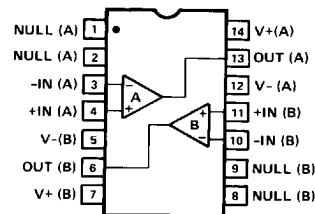
The OP-207 series of dual matched operational amplifiers consists of two independent OP-07 high performance operational amplifiers in a single 14-pin dual-in-line package. Exceptionally low offset voltage and tight matching of critical

parameters is provided between the channels of this dual operational amplifier.

The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels provide high performance in instrumentation amplifier designs. The individual amplifiers feature very low input offset voltage, low offset voltage drift, low noise voltage, and low bias current. Each amplifier is fully compensated and protected.

Matching between channels is provided on all critical parameters including offset voltage, tracking of offset voltage vs. temperature, noninverting bias currents, and common-mode rejection.

### PIN CONNECTIONS

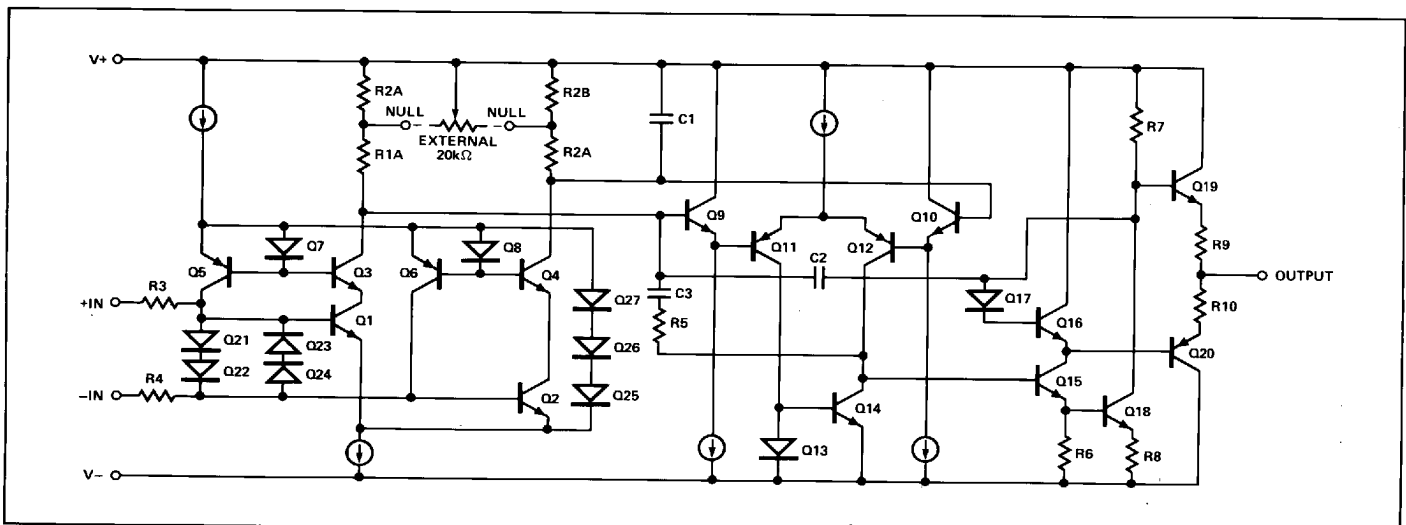


**14-PIN HERMETIC DIP  
(Y-Suffix)**

#### NOTES:

1. Device may be operated even if insertion is reversed; this is due to inherent symmetry of pin locations of amplifiers A and B.
2. V-(A) and V-(B) are internally connected via substrate resistance.

### SIMPLIFIED SCHEMATIC (1/2 OP-207)



## ABSOLUTE MAXIMUM RATINGS

Supply Voltage .....	±22V
Differential Input Voltage .....	±30V
Input Voltage (Note 1) .....	±22V
Output Short-Circuit Duration .....	Indefinite
Storage Temperature Range .....	-65°C to 150°C
Operating Temperature Range	
OP-207A .....	-55°C to +125°C
OP-207E, OP-207F .....	0°C to +70°C
Lead Temperature (Soldering, 60 sec) .....	300°C

PACKAGE TYPE	$\theta_{JA}$ (Note 2)	$\theta_{JC}$	UNITS
14-Pin Hermetic DIP (Y)	108	16	°C/W

### NOTES:

1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2.  $\theta_{JA}$  is specified for worst case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for CerDIP package.

## MATCHING CHARACTERISTICS at $V_S = \pm 15V$ , $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207A/E			OP-207F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	$\Delta V_{OS}$	$R_S = 100\Omega$	—	30	90	—	50	280	$\mu V$
Average Noninverting Bias Current	$I_{B^+}$		—	±1.5	±3.5	—	±1.5	±6.0	nA
Noninverting Offset Current	$I_{OS^+}$		—	±0.7	±3.5	—	±1.0	±6.0	nA
Inverting Offset Current	$I_{OS^-}$		—	±0.7	±3.5	—	±1.0	±6.0	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	103	120	—	96	114	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	$\mu V/V$
Channel Separation			126	140	—	126	140	—	dB

## MATCHING CHARACTERISTICS at $V_S = \pm 15V$ , $-55^\circ C \leq T_A \leq 125^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207A			UNITS
			MIN	TYP	MAX	
Input Offset Voltage Match	$\Delta V_{OS}$	$R_S = 100\Omega$	—	70	180	$\mu V$
Input Offset Voltage Tracking						
Without External Trim	$TC\Delta V_{OS}$	(Note 1)	—	0.5	1.0	$\mu V/^\circ C$
With External Trim	$TC\Delta V_{OSn}$	$R_p = 20k\Omega$ (Note 1)	—	0.3	1.0	$\mu V/^\circ C$
Average Noninverting Bias Current	$I_{B^+}$		—	±2	±6	nA
Average Drift of Non-inverting Bias Current	$TCI_{B^+}$		—	10	—	$pA/^\circ C$
Noninverting Offset Current	$I_{OS^+}$		—	2	6.5	nA
Average Drift of Non-inverting Offset Current	$TCI_{OS^+}$		—	12	—	$pA/^\circ C$
Inverting Offset Current	$I_{OS^-}$		—	2	6.5	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	100	117	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	10	51	$\mu V/V$

### NOTE:

1. Sample tested.

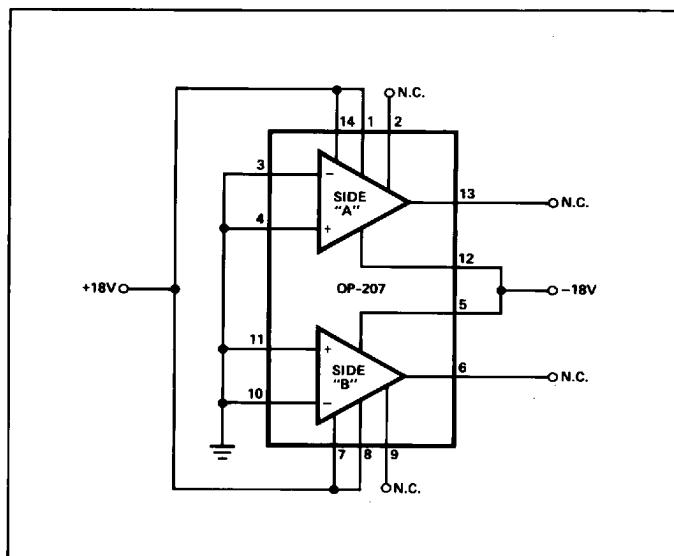
**MATCHING CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $0^\circ C \leq T_A \leq 70^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207E			OP-207F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	$\Delta V_{OS}$	$R_S = 100\Omega$	—	60	150	—	120	350	$\mu V$
Input Offset Voltage Tracking									
Without External Trim	$TC\Delta V_{OS}$	(Note 1)	—	0.5	1.0	—	0.9	1.5	$\mu V/^\circ C$
With External Trim	$TC\Delta V_{OSn}$	$R_P = 20k\Omega$ (Note 1)	—	0.3	1.0	—	0.4	1.3	$\mu V/^\circ C$
Average Noninverting Bias Current	$I_{B+}$		—	$\pm 2$	$\pm 5$	—	$\pm 3$	$\pm 10$	nA
Average Drift of Non-inverting Bias Current	$TCI_{B+}$		—	10	—	—	12	—	$pA/^\circ C$
Noninverting Offset Current	$I_{OS+}$		—	2	5	—	3	10	nA
Average Drift of Non-inverting Offset Current	$TCI_{OS+}$		—	12	—	—	15	—	$pA/^\circ C$
Inverting Offset Current	$I_{OS-}$		—	2	5	—	3	10	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	100	117	—	94	114	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	10	51	—	16	100	$\mu V/V$

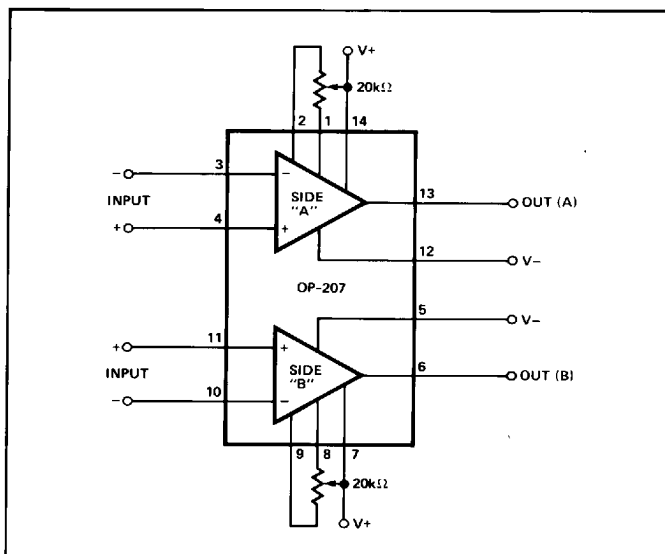
**NOTE:**

1. Sample tested.

**BURN-IN CIRCUIT**



**OFFSET NULLING CIRCUIT**



**INDIVIDUAL AMPLIFIER CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207A/E			OP-207F			UNITS
			MIN	TYP	MAX	MIN	TYP*	MAX	
Input Offset Voltage	$V_{OS}$	$R_S = 100\Omega$	—	35	100	—	60	200	$\mu V$
Input Offset Voltage Stability	$\Delta V_{OS}/\text{Time}$	(Note 1)	—	0.3	1.5	—	0.4	2.0	$\mu V/Mo$
Input Offset Current	$I_{OS}$		—	0.9	2.8	—	1.5	6.0	nA
Input Bias Current	$I_B$		—	$\pm 1$	$\pm 3$	—	$\pm 2$	$\pm 7$	nA
Input Noise Voltage	$e_{np-p}$	0.1Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.35	0.6	$\mu V_{p-p}$
Input Noise Voltage Density	$e_n$	$f_O = 10\text{Hz}$ (Note 2)	—	10.3	18.0	—	10.3	18.0	$nV/\sqrt{Hz}$
		$f_O = 100\text{Hz}$ (Note 2)	—	10.0	13.0	—	10.0	13.0	
		$f_O = 1000\text{Hz}$ (Note 2)	—	9.6	—	—	9.6	—	
Input Noise Current	$I_{np-p}$	0.1Hz to 10Hz (Note 2)	—	14	30	—	14	30	$pA_{p-p}$
Input Noise Current Density	$I_n$	$f_O = 10\text{Hz}$ (Note 2)	—	0.32	0.80	—	0.32	0.80	$pA/\sqrt{Hz}$
		$f_O = 100\text{Hz}$ (Note 2)	—	0.14	0.23	—	0.14	0.23	
		$f_O = 1000\text{Hz}$ (Note 2)	—	0.12	—	—	0.12	—	
Input Resistance — Differential Mode	$R_{IN}$	(Note 3)	20	60	—	8	30	—	M $\Omega$
Input Resistance — Common-Mode	$R_{IN CM}$		—	200	—	—	120	—	G $\Omega$
Input Voltage Range	IVR		$\pm 13$	$\pm 14$	—	$\pm 13$	$\pm 14$	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	7	32	$\mu V/V$
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ , $V_O = \pm 10V$	200	500	—	150	400	—	V/mV
Output Voltage Swing	$V_O$	$R_L \geq 10k\Omega$	$\pm 12.5$	$\pm 13.0$	—	$\pm 12.5$	$\pm 13.0$	—	V
		$R_L \geq 2k\Omega$	$\pm 12.0$	$\pm 12.8$	—	$\pm 12.0$	$\pm 12.8$	—	
		$R_L \geq 1k\Omega$	$\pm 10.0$	$\pm 12.0$	—	$\pm 10.0$	$\pm 12.0$	—	
Slew Rate	SR	$R_L \geq 2k\Omega$	—	0.2	—	—	0.2	—	V/ $\mu s$
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	—	0.6	—	—	0.6	—	MHz
Open-Loop Output Resistance	$R_O$	$V_O = 0$ , $I_O = 0$	—	60	—	—	60	—	$\Omega$
Power Consumption	$P_d$	No Load, Both Amplifiers	—	180	240	—	200	300	mW
Offset Adjustment Range		$R_P = 20k\Omega$	—	$\pm 4$	—	—	$\pm 4$	—	mV
Input Capacitance	$C_{IN}$		—	8	—	—	8	—	pF

**NOTES:**

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of  $V_{OS}$  vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in  $V_{OS}$  during the first 30 operating days are typically  $2.5\mu V$ . Parameter is sample tested.
2. Sample tested.
3. Guaranteed by design.

**INDIVIDUAL AMPLIFIER CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $-55^\circ C \leq T_A \leq 125^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207A			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$	$R_S = 100\Omega$	—	75	230	$\mu V$
Average Input Offset Voltage Drift						
Without External Trim	$TCV_{OS}$	$R_P = 20k\Omega$ (Notes 1, 2)	—	0.4	1.3	$\mu V/^\circ C$
With External Trim	$TCV_{OSn}$		—	0.4	—	
Input Offset Current	$I_{OS}$		—	1.8	5.6	nA
Average Input Offset Current Drift	$TCI_{OS}$		—	10	—	$pA/^\circ C$
Input Bias Current	$I_B$		—	$\pm 3.0$	$\pm 5.6$	nA
Average Input Bias Current Drift	$TCI_B$		—	12	—	$pA/^\circ C$
Input Voltage Range	IVR		$\pm 13$	$\pm 13.5$	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	$\mu V/V$
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ , $V_O = \pm 10V$	150	400	—	V/mV
Output Voltage Swing	$V_O$	$R_L \geq 2k\Omega$	$\pm 12.0$	$\pm 12.8$	—	V

**INDIVIDUAL AMPLIFIER CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $0^\circ C \leq T_A \leq 70^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207E			OP-207F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$	$R_S = 100\Omega$	—	60	200	—	90	350	$\mu V$
Average Input Offset Voltage Drift									
Without External Trim	$TCV_{OS}$	$R_P = 20k\Omega$ (Notes 1, 2)	—	0.4	1.3	—	0.7	1.8	$\mu V/^\circ C$
With External Trim	$TCV_{OSn}$		—	0.4	—	—	0.7	—	
Input Offset Current	$I_{OS}$		—	1.4	5	—	2.5	10	nA
Average Input Offset Current Drift	$TCI_{OS}$		—	10	—	—	12	—	$pA/^\circ C$
Input Bias Current	$I_B$		—	$\pm 2$	$\pm 5$	—	$\pm 3$	$\pm 11$	nA
Average Input Bias Current Drift	$TCI_B$		—	12	—	—	18	—	$pA/^\circ C$
Input Voltage Range	IVR		$\pm 13$	$\pm 13.5$	—	$\pm 13$	$\pm 13.5$	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	120	—	97	117	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	$\mu V/V$
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ , $V_O = \pm 10V$	150	400	—	120	350	—	V/mV
Output Voltage Swing	$V_O$	$R_L \geq 2k\Omega$	$\pm 12.0$	$\pm 12.8$	—	$\pm 12.0$	$\pm 12.8$	—	V

**NOTES:**

- Exclude first hour of operation to allow for stabilization of external circuitry.
- Sample tested.

## APPLICATION OF DUAL MATCHED OPERATIONAL AMPLIFIERS

### ADVANTAGES OF DUAL MATCHED OPERATIONAL AMPLIFIERS

Dual matched operational amplifiers provide a powerful tool for the solution of some difficult circuit design problems. Circuits include true instrumentation amplifiers, extremely low drift, high common-mode rejection DC amplifiers, low DC drift active filters, dual tracking voltage references, and many other demanding applications. These designs all require good matching between two operational amplifiers.

The circuit below, a differential-in, differential-out amplifier, shows how errors can be reduced. Assuming the resistors used are matched, the gain of each side will be identical; if the offset voltage of each amplifier is matched, then the net differential voltage at the amplifiers output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the *difference* between the amplifiers' offset voltages. This error-cancellation principle holds for a number of input-referred error parameters — offset voltage, offset voltage drift, inverting and noninverting bias currents,

common-mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential-mode, are extremely high, an important feature not possible with single operational amplifier circuits. Common-mode rejection can be made exceptionally high; this is very important in instrumentation amplifiers where errors due to large common-mode voltages can be far greater than errors due to noise or drift with temperature. For example, consider the case of two op amps, each with 80dB (100 $\mu$ V/V) CMRR. If the CMRR of one device is +100 $\mu$ V/V CMRR and the other is -100 $\mu$ V/V, then the net CMRR will be 200 $\mu$ V/V, a 6dB degradation. The matching of CMRR increases the effective CMRR when used as an instrumentation input stage.

### POWER SUPPLIES

The V+ supply terminals are completely independent and may be powered by separate supplies if desired. However, this approach would sacrifice the advantages of the power-supply-rejection-ratio matching. The V- supply terminals are both connected to the common substrate and must be tied to the same voltage.

### OFFSET TRIMMING

Offset voltage trimming is provided for each amplifier. Guaranteed performance over temperature is obtained by trimming one side (side A) to match the offset of the other. A net differential offset of zero results. This procedure is used during factory testing of the devices. The same results are obtained by trimming side B to match side A or by nulling each side individually.

The OP-207 is designed to provide best drift performance when trimmed with a 20k $\Omega$  potentiometer; this value provides about  $\pm 4$ mV of adjustment range which is adequate for most applications. Trimming resolution can be increased by use of the circuit shown below.

