PRELIMINARY

MOSTEK®

1K x 8 STATIC RAM

MK4118(P/J/N) Series

FEATURES

- Address Activated™ Interface combines benefits of Edge Activated™ and fully static operation
- High performance

Part Number	Access Time	Cycle Time
MK4118-1	120 nsec	120 nsec
MK4118-2	150 nsec	150 nsec
MK4118-3	200 nsec	200 nsec
MK4118-4	250 nsec	250 nsec

- Single +5 volt power supply
- TTL compatible I/O
  Fanout: 2 - Standard TTL
  2 - Schottky TTL
  12 - Low power Schottky TTL
- Low Power - 400mw Active
- $\overline{CE}$, $\overline{OE}$, and $\overline{LATCH}$ functions for flexible system operation
- Pin compatible with Mostek's BYTEWYDE™ memory family

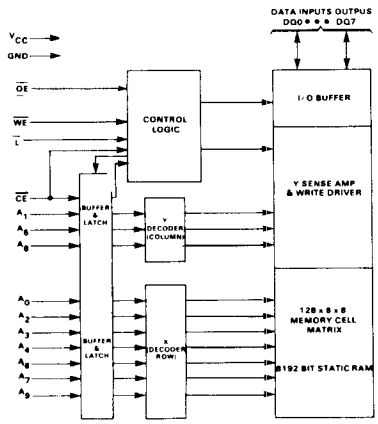
DESCRIPTION

The MK4118 uses Mostek's Poly R N-Channel Silicon Gate process and advanced circuit design techniques to package 8192 bits of static RAM on a single chip. Mostek's Address Activated™ circuit design technique is utilized to achieve high performance, low power, and easy user implementation. The device has a V_{IH} = 2.2, V_{IL} = 0.8V, V_{OH} = 2.4, V_{OL} = 0.4V making it totally compatible with all TTL family devices.

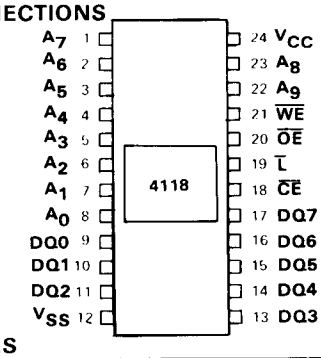
The MK4118 is designed for all wide word memory applications. The MK4118 provides the user with a high-density, cost-effective 1K x 8-bit Random Access Memory. Fast Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls are provided for easy interface in microprocessor or other bus-oriented systems. The MK4118 features a flexible Latch ($\overline{L}$) function to permit latching of the address and $\overline{CE}$ status at the user's option. Common data and address bus operation may be performed at the system level by utilizing the $\overline{L}$ and $\overline{OE}$ functions for the MK4118. The latch function may be bypassed by merely tying the latch pin to V_{CC}, providing fast ripple-through operation.

STATIC RAMS

BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES

A0-A9	Address Inputs	$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable	$\overline{OE}$	Output Enable
V_{SS}	Ground	$\overline{L}$	Latch
V_{CC}	Power (+5V)	DQ_0 - DQ_7	Data In/ Data Out

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -0.5V to +7.0V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ambient) (Ceramic) ..... -65°C to +150°C
Storage Temperature (Ambient) (Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 20mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[3]

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2		7.0	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3		0.8	V	1

DC ELECTRICAL CHARACTERISTICS[1,3]

($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0 volts ± 5%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current (Active)		80	mA	7
I_{CC2}	Average V_{CC} Power Supply Current (Standby)		60	mA	5
I_{IL}	Input Leakage Current (Any Input)	-10	10	μA	2
I_{OL}	Output Leakage Current	-10	10	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1mA	2.4		V	
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA		0.4	V	

AC ELECTRICAL CHARACTERISTICS[1,3]

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 5%)

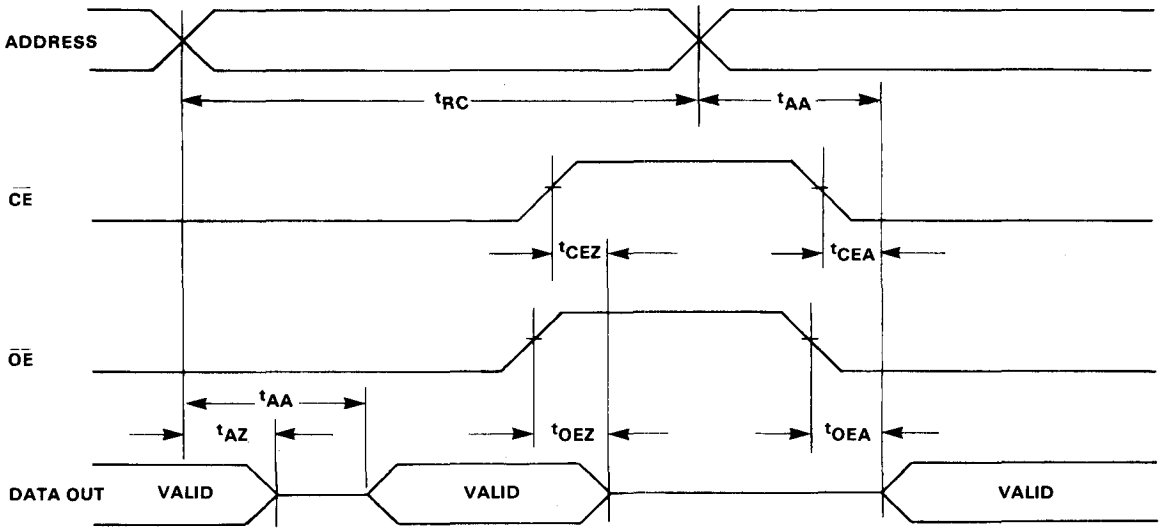
SYM	PARAMETER	TYP	MAX	NOTES
C_I	Capacitance on all pins except I/O	4pF		4
$C_{I/O}$	Capacitance on I/O pins	10pF		4

NOTES:
1. All voltages reference to V_{SS}.
2. Measured with $0 \leq V_I \leq 5V$ and outputs deselected (V_{CC} = 5V)
3. A minimum of 2msec time delay is required after application of V_{CC} (+5V) before proper device operation can be achieved.
4. Effective capacitance calculated from the equation $C = I \frac{\Delta t}{\Delta V}$ with $\Delta V = 3V$ and V_{CC} nominal.
5. Standby mode is defined as condition with addresses, latch and $\overline{WE}$ remain unchanged.
6. AC timing measurements made with 2 TTL loads plus 100pF.
7. I_{CC} active measured with outputs open.

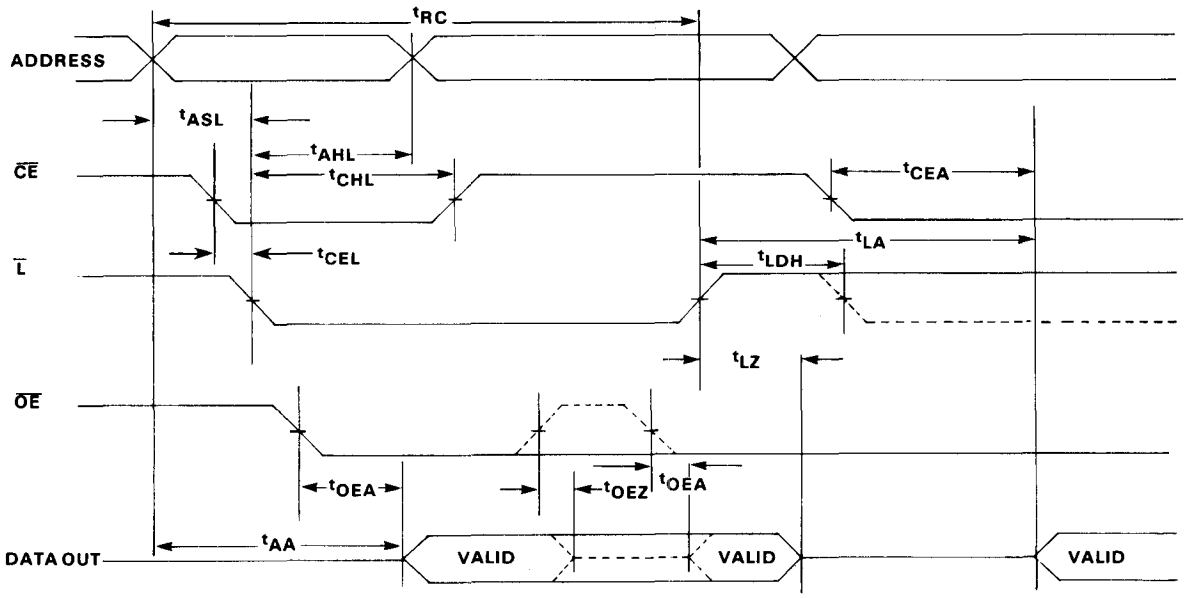
ELECTRICAL CHARACTERISTICS[6]
($0°C \leq T_A \leq 70°C$ and $V_{CC} = 5.0$ volts $\pm$ 5%)

		MK4118-1		MK4118-2		MK4118-3		MK4118-4			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT	NOTE
t_{RC}	Read Cycle Time	120		150		200		250		ns	
t_{AA}	Address Access Time		120		150		200		250	ns	
t_{CEA}	Chip Enable Access Time		60		75		100		125	ns	
t_{CEZ}	Chip Enable Data Off Time	0	60	0	75	0	100	0	125	ns	
t_{OEA}	Output Enable Access Time		60		75		100		125	ns	
t_{OEZ}	Output Enable Data Off Time	0	60	0	75	0	100	0	125	ns	
t_{AZ}	Address Data Off Time	10		10		10		10		ns	
t_{ASL}	Address to Latch Setup Time	10		10		10		20		ns	
t_{AHL}	Address From Latch Hold Time	40		50		65		80		ns	
t_{CEL}	$\overline{CE}$ to Latch Setup Time	0		0		0		0		ns	
t_{CHL}	$\overline{CE}$ From Latch Hold Time	40		50		65		80		ns	
t_{LA}	Latch Off Access Time		155		200		260		320	ns	
t_{WC}	Write Cycle Time	120		150		200		250		ns	
t_{ASW}	Address To Write Setup Time	0		0		0		0		ns	
t_{AHW}	Address From Write Hold Time	40		50		65		80		ns	
t_{CEW}	$\overline{CE}$ To Write Setup Time	0		0		0		0		ns	
t_{CHW}	$\overline{CE}$ From Write Hold Time	40		50		65		80		ns	
t_{DSW}	Data To Write Setup Time	20		30		40		50		ns	
t_{DHW}	Data From Write Hold Time	20		30		40		50		ns	
t_{WD}	Write Pulse Duration	35		50		60		70		ns	
t_{LDH}	Latch Duration, High	35	DC	50	DC	60	DC	70	DC	ns	
t_{LDL}	Latch Duration, Low		DC		DC		DC		DC	ns	
t_{WEZ}	Write Enable Data Off Time	0	60	0	75	0	100	0	125	ns	
t_{LZ}	Latch Data Off Time	10		10		10		10		ns	
t_{WPL}	Write Pulse Lead Time	75		90		130		170		ns	

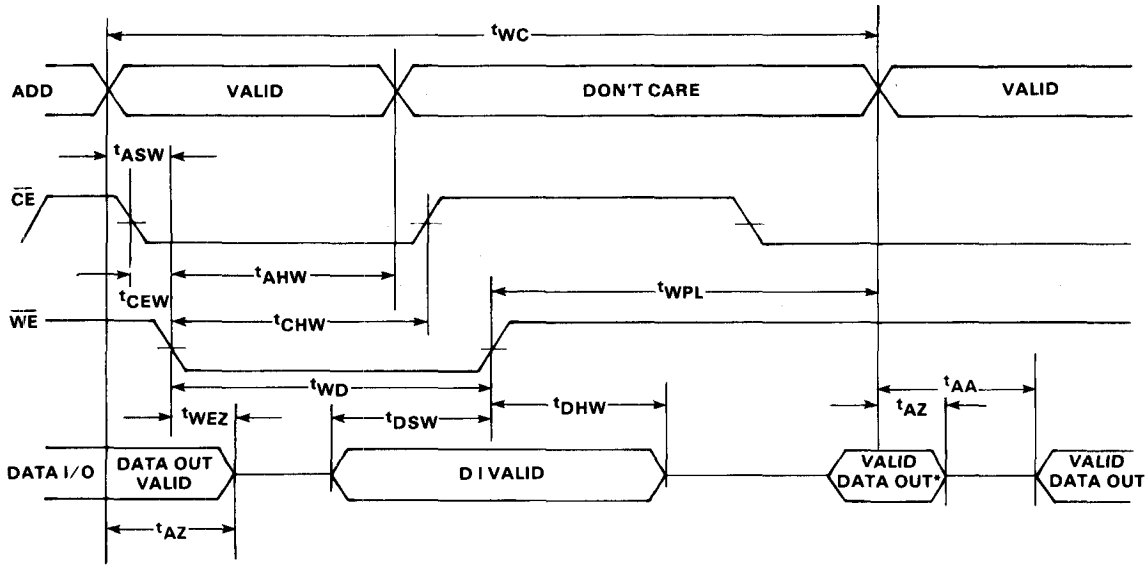
STATIC READ CYCLE
$\overline{WE}$ = $\overline{L}$ = HIGH



LATCHED READ CYCLE
$\overline{WE}$ = HIGH



WRITE CYCLE
$\overline{OE}$ = LOW, $\overline{L}$ = HIGH



OPERATION

READ MODE

The MK4118 is in the READ MODE whenever the Write Enable control input ($\overline{WE}$) is in the high state. The state of the 8 data I/O signals is controlled by the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) control signals. The READ MODE memory cycle may be either STATIC (ripple-through) or LATCHED, depending on user control of the Latch Input Signal ($\overline{L}$).

STATIC READ CYCLE

In the STATIC READ CYCLE mode of operation, the MK4118 provides a fast address ripple-through access of data from 8 of 8192 locations in the static storage array. Thus, the unique address specified by the 10 Address Inputs (An) define which 1 of 1024 bytes of data is to be accessed. The STATIC READ CYCLE is defined by $\overline{WE}$ = $\overline{L}$ = High.

A transition on any of the 10 address inputs will disable the 8 Data Output Drivers after t_{AZ}. Valid Data will be available to the 8 Data Output Drivers with t_{AA} after all address input signals are stable, and the data will be output under control of the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) signals.

LATCHED READ CYCLE

The LATCHED READ CYCLE is also defined by the Write Enable control input ($\overline{WE}$) being in the high state, and it is synchronized by proper control of the Latch ($\overline{L}$) input.

As the Latch control input ($\overline{L}$) is taken low, Address (An) and Chip Enable ($\overline{CE}$) inputs that are stable for the specified set-up and hold times are latched internally. Data out corresponding to the latched address will be supplied to the Data Output drivers. The output drivers will be enabled to drive the Output Data Bus under control of the Output Enable ($\overline{OE}$) and latched Chip Enable ($\overline{CE}$) inputs.

Taking the latch input high begins another read cycle for the memory locations specified by the address then appearing on the Address Input (An). Returned the latch control to the low state latches the new Address and Chip Enable inputs internally for the remainder of the LATCHED READ CYCLE.

NOTE: If the 'LATCH' function is not used pin 19 ($\overline{L}$) must be tied high (V_{IH} min).

WRITE MODE

The MK4118 is in the WRITE MODE whenever the Write Enable ($\overline{WE}$) and Chip Enable ($\overline{CE}$) control inputs are in the low state. The status of the 8 output buffers during a write cycle is explained below.

WRITE MODE (Cont'd)

The WRITE cycle is initiated by the $\overline{WE}$ pulse going low provided that $\overline{CE}$ is also low. The leading edge of the $\overline{WE}$ pulse is used to latch the status of the address bus. $\overline{CE}$ if active (Low) will also be latched. NOTE: $\overline{WE}$ is gated by $\overline{CE}$. If $\overline{CE}$ goes low after $\overline{WE}$, the Write Cycle will be initiated by $\overline{CE}$, and all timing will be referenced to that edge. $\overline{CE}$ and the Addresses will then be latched, and the cycle must be terminated by $\overline{WE}$ going high. The output bus if not already disabled will go to the high Z state t_{WEZ} after $\overline{WE}$. The latch signal, if at a logic high, will have no impact on the WRITE cycle. If latch is brought from a logic high to low prior to $\overline{WE}$ going active then the address inputs and $\overline{CE}$ will be latched. NOTE: The Latch control ($\overline{L}$) will latch $\overline{CE}$ independent of the state, whereas $\overline{WE}$ will latch $\overline{CE}$ only when in the low state. Once latched, $\overline{CE}$ and the address inputs may be removed after the required hold times have been met.

Data in must be valid t_{DSW} prior to the low-to-high transition of $\overline{WE}$. The Data in lines must remain stable for t_{DHW} after $\overline{WE}$ goes inactive. The write control of the MK4118 disables the data out buffers during the write cycle; however, output enable ($\overline{OE}$) should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.