Document Number: MC34119
Rev. 3.0, 12/2006

Low Power Audio Amplifier

The 34119 is a low power audio amplifier integrated circuit intended for telephone applications, such as in speakerphones. It provides differential speaker outputs to maximize output swing at low supply voltages (2.0 V minimum). Coupling capacitors to the speaker are not required. Open loop gain is 80 dB, and the closed loop gain is set with two external resistors. A Chip Disable pin permits powering down and/or muting the input signal.

Features

- Wide Operating Supply Voltage Range (2.0 V to 16 V), Allows Telephone Line Powered Applications
- Low Quiescent Supply Current (2.7 mA Typ) for Battery Powered Applications
- Chip Disable Input to Power Down the IC
- Low Power--Down Quiescent Current (65 µA Typ)
- Drives a Wide Range of Speaker Loads (8.0 Ω and Up)
- Output Power Exceeds 250 mW with 32 Ω Speaker
- Low Total Harmonic Distortion (0.5% Typ)
- Gain Adjustable from <0 dB to >46 dB for Voice Band
- Requires Few External Components
- Pb-Free Packaging Designated by Suffix Code EF

34119

LOW POWER AUDIO AMPLIFIER

D SUFFIX
EF SUFFIX (PB-FREE)
98ASB42564B
8-PIN SOICN

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC34119D/R2	-20°C to 70°C	8 SOICN
MCZ34119EF/R2		

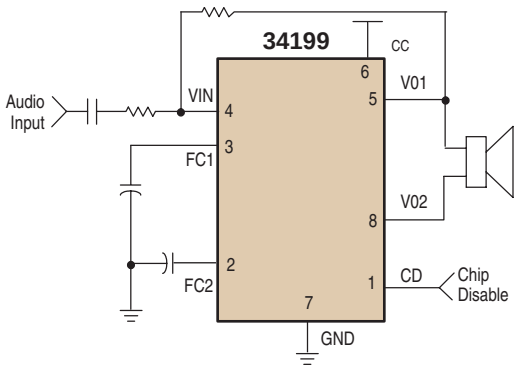


Figure 1. 34119 Simplified Application Diagram

INTERNAL BLOCK DIAGRAM

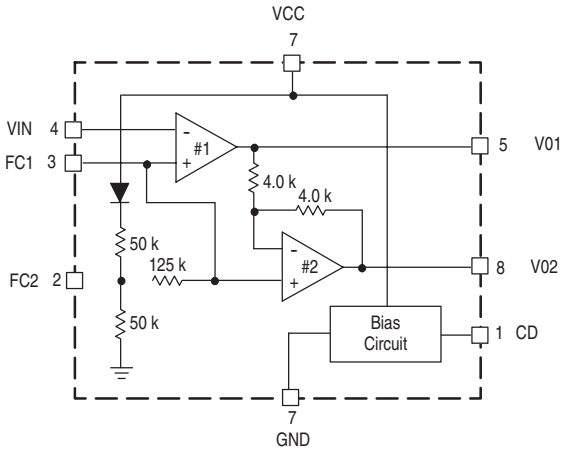


Figure 2. 34119 Simplified Internal Block Diagram

PIN CONNECTIONS

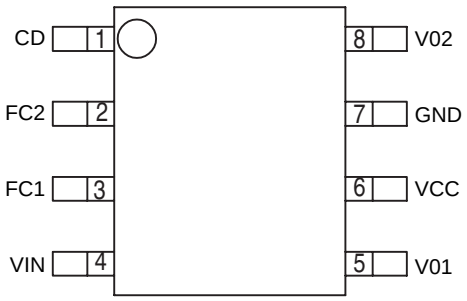


Figure 3. 34119 Pin Connections

Table 1. 34119 Pin Definitions

Pin Number	Pin Name	Definition
1	CD	Chip Disable -- Digital input. A Logic “0” (<0.8 V) sets normal operation. A logic “1” (≥2.0 V) sets the power down mode. Input impedance is nominally 90 kΩ.
2	FC2	A capacitor at this pin increases power supply rejection, and affects turn--on time. This pin can be left open if the capacitor at FC1 is sufficient.
3	FC1	Analog ground for the amplifiers. A 1.0 μF capacitor at this pin (with a 5.0 μF capacitor at Pin 2) provides (typically) 52 dB of power supply rejection. Turn--on time of the circuit is affected by the capacitor on this pin. This pin can be used as an alternate input.
4	VIN	Amplifier input. The input capacitor and resistor set low frequency rolloff and input impedance. The feedback resistor is connected to this pin and VO1.
5	V01	Amplifier Output #1. The dc level is ≈ (VCC - 0.7 V)/2.
6	VCC	DC supply voltage (+2.0 V to +16 V) is applied to this pin.
7	GND	Ground pin for the entire circuit.
8	V02	Amplifier Output #2. This signal is equal in amplitude, but 180° out--of--phase with that at VO1. The dc level is ≈ (VCC -- 0.7 V)/2.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Min	Max	Unit
ELECTRICAL RATINGS				
Supply Voltage Voltage @ CD (Pin 1)	V_{CC} V_{CD}	2.0 0.0	16 V_{CC}	V_{DC} V_{DC}
Load Impedance (at V_{IN})	R_L	8.0	-	Ω
Peak Load Current	IL	-	±200	mA
Differential Gain (5.0 kHz Bandwidth)	AVD	0.0	46	dB
THERMAL RATINGS				
Ambient Temperature	TA	-20	70	°C
THERMAL RESISTANCE				
Peak Package Reflow Temperature During Reflow (1), (2)	T_{PPRT}	Note 2		°C

Notes

1. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
2. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
   Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions -1.0 V ≤ V_{CC} ≤ 18 V, -20°C ≤ T_A ≤ 70°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
AMPLIFIERS					
Output DC Level @ VO1, VO2, VCC = 3.0 V, R_L = 16 (R_F = 75 k)	$V_{O(3)}$	1.0	1.15	1.25	V
V_{CC} = 6.0 V	$V_{O(6)}$	-	2.65	-	
V_{CC} = 12 V	$V_{O(12)}$	-	5.65	-	
Output Level					V
High (I_{OUT} = -75 mA, 2.0 V ≤ V_{CC} ≤ 16 V)	V_{OH}	-	V_{CC} - 1.0	-	
Low (I_{OUT} = 75 mA, 2.0 V ≤ V_{CC} ≤ 16 V)	V_{OL}	-	0.16	-	
Output DC Offset Voltage (VO1 - VO2)	ΔV_O				mV
(V_{CC} = 6.0 V, R_F = 75 kΩ, R_L = 32Ω)		-30	0.0	30	
Input Bias Current @ V_{IN} (V_{CC} = 6.0 V)	I_{IB}	-	-100	-200	nA
Equivalent Resistance					kΩ
@ FC1 (VCC = 6.0 V)	R_{FC1}	100	150	220	
@ FC2 (VCC = 6.0 V)	R_{FC2}	18	25	40	
CHIP DISABLE					
Input Voltage					V
Low	V_{IL}	-	-	0.8	
High	V_{IH}	2.0	-	-	
Input Resistance (V_{CC} = V_{CD} = 16 V)	R_{CD}	50	90	175	kΩ
POWER SUPPLY					
Power Supply Current					
(V_{CC} = 3.0 V, R_L = ∞, CD = 0.8 V)	I_{CC3}	-	2.7	4.0	mA
(V_{CC}= 16 V, R_L = ∞, CD = 0.8 V)	I_{CC16}	-	3.3	5.0	mA
(V_{CC} = 3.0 V, R_L = ∞, CD = 2.0 V)	I_{CCD}	-	65	100	μA
TYPICAL TEMPERATURE PERFORMANCE (-20°C < T_A < 70°C)					
Input Bias Current @ V_{IN}	I_{IN}	-	±40	-	pA/°C
Total Harmonic Distortion	T_{HD}	-	±0.003	-	**%/°C**
(V_{CC} = 6.0 V, R_L = 32Ω, P_{OUT} = 125 mW, f = 1.0 kHz)					
Power Supply Current	I_{CC}				μA/°C
(V_{CC} = 3.0 V, R_L = ∞, CD = 0 V		-	-2.5	-	
(V_{CC} = 3.0 V, R_L = ∞, CD = 2.0 V)		-	-0.03	-	

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions -1.0 V ≤ V_{CC} ≤ 18 V, -20°C ≤ T_A ≤ 70°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
AMPLIFIERS					
AC Input Resistance (@ V_{IN})	R_I	-	> 30	-	MΩ
Open Loop Gain (Amplifier #1, f < 100 Hz)	A_{VOL1}	80	-	-	dB
Closed Loop Gain (Amplifier #2, V_{CC} = 6.0 V, f = 1.0 kHz, R_L = 32Ω)	A_V2	-0.35	0.0	0.35	dB
Gain Bandwidth Product	GBW	-	1.5	-	MHz
Output Power					mW
V_{CC} = 3.0 V, R_L = 16Ω, THD ≤ 10%	P_{OUT3}	55	-	-	
V_{CC} = 6.0 V, R_L = 32Ω, THD ≤ 10%	P_{OUT6}	240	-	-	
V_{CC} = 12 V, R_L = 100Ω, THD ≤ 10%%	P_{OUT12}	400	-	-	
Total Harmonic Distortion (f = 1.0 kHz)	THD				%
(V_{CC} = 6.0 V, R_L = 32Ω, P_{OUT} = 125 mW)		-	0.5	1.0	
(V_{CC} ≥ 3.0 V, R_L = 8.0Ω, P_{OUT} = 20 mW)		-	0.5	-	
(V_{CC} ≥ 12 V, R_L = 32Ω, P_{OUT} = 200 mW)		-	0.6	-	
Power Supply Rejection (V_{CC} = 6.0 V, ΔV_{CC} = 3.0 V)	PSRR				dB
(C1 = ∞, C2 = 0.01 μF)		50	-	-	
(C1 = 0.1 μF, C2 = 0, f = 1.0 kHz)		-	12	-	
(C1 = 1.0 μF, C2 = 5.0 μF, f = 1.0 kHz)		-	52	-	
Differential Muting (V_{CC} = 6.0 V, 1.0 kHz ≤ f ≤ 20 kHz, CD = 2.0 V)	GMT	-	> 70	-	dB

ELECTRICAL PERFORMANCE CURVES

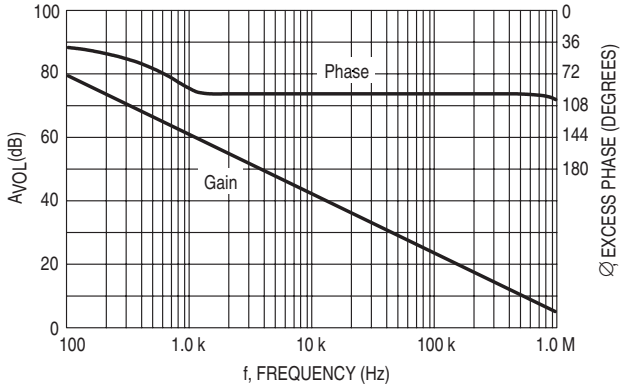


Figure 4. Amplifier #1 Open Loop Gain and Phase

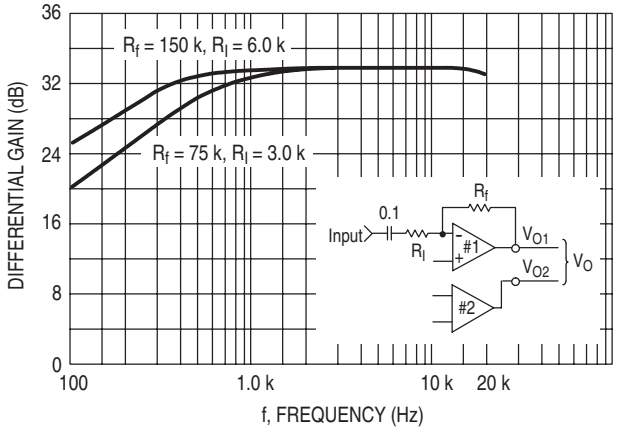


Figure 5. Differential Gain versus Frequency

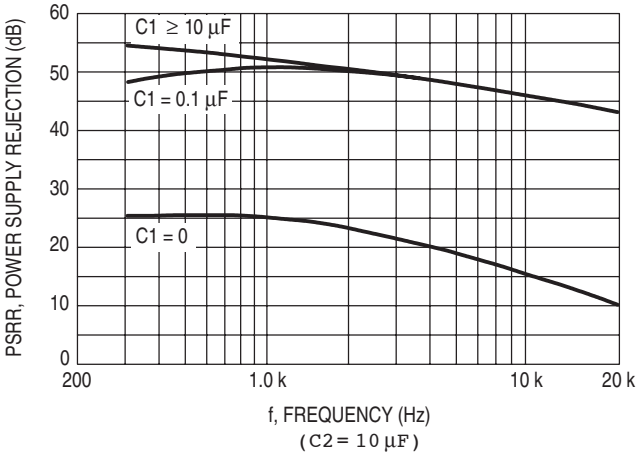


Figure 6. Power Supply Rejection versus Frequency

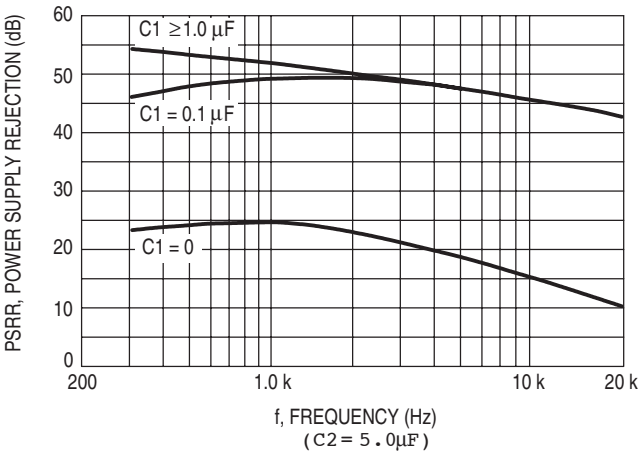


Figure 7. Power Supply Rejection versus Frequency

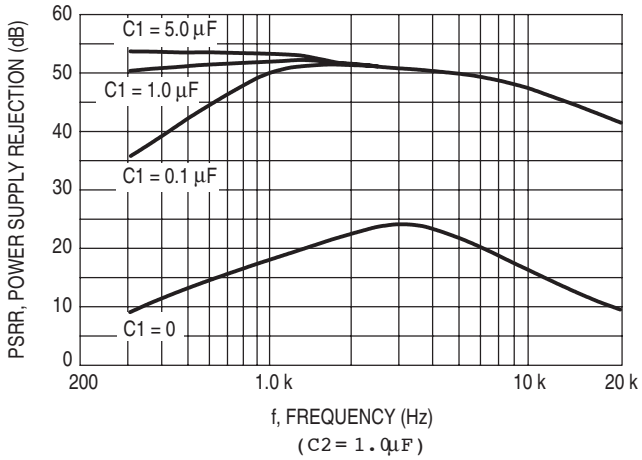


Figure 8. Power Supply Rejection versus Frequency

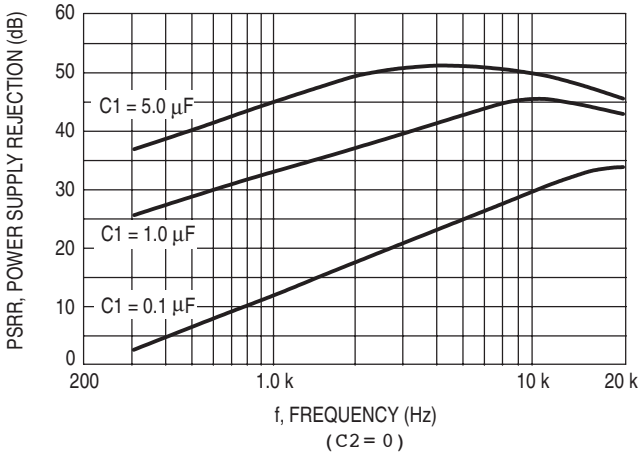


Figure 9. Power Supply Rejection versus Frequency

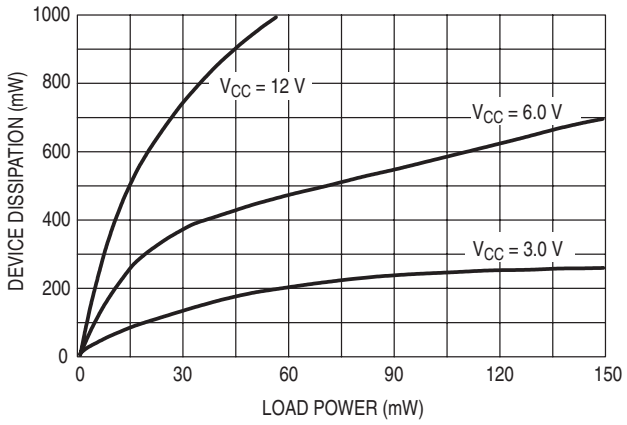


Figure 10. Device Dissipation, 8.0Ω Load

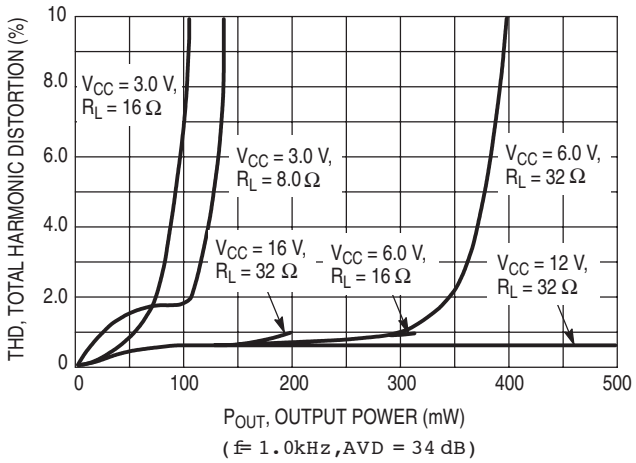


Figure 13. Distortion versus Power

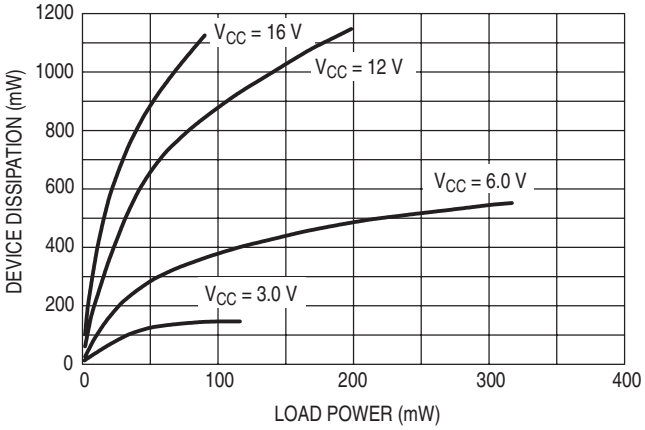


Figure 11. Device Dissipation, 16 Ω Load

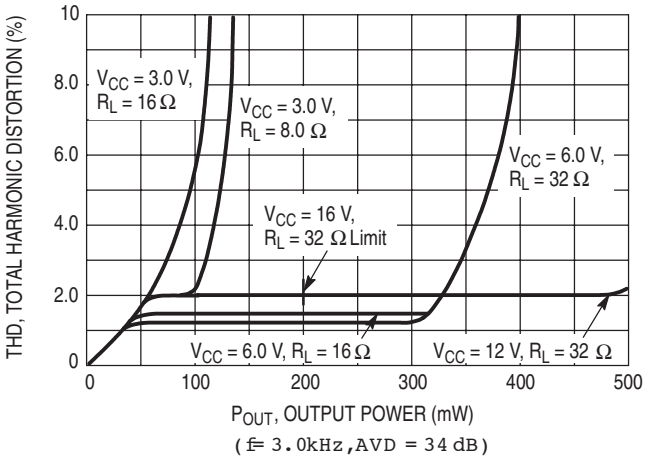


Figure 14. Distortion versus Power

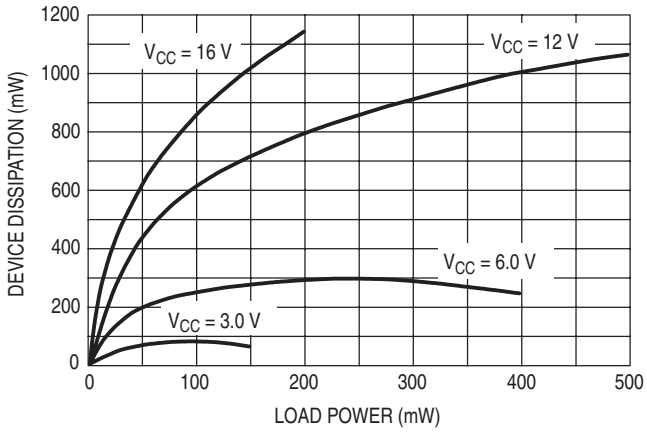


Figure 12. Device Dissipation, 32 Ω Load

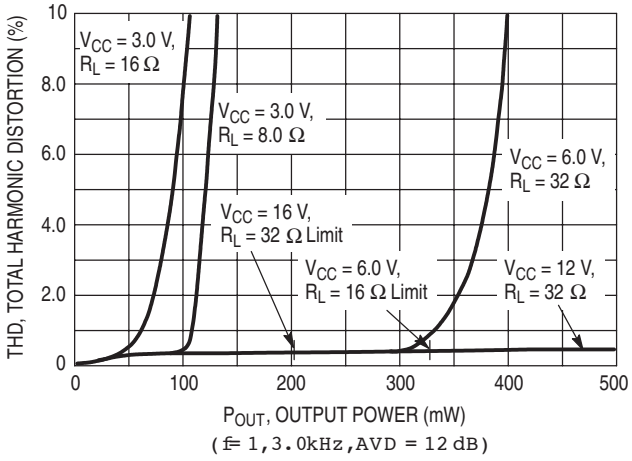


Figure 15. Distortion versus Power

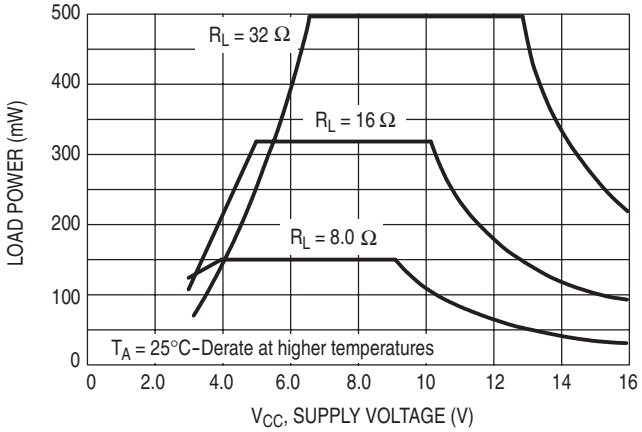


Figure 16. Maximum Allowable Load Power

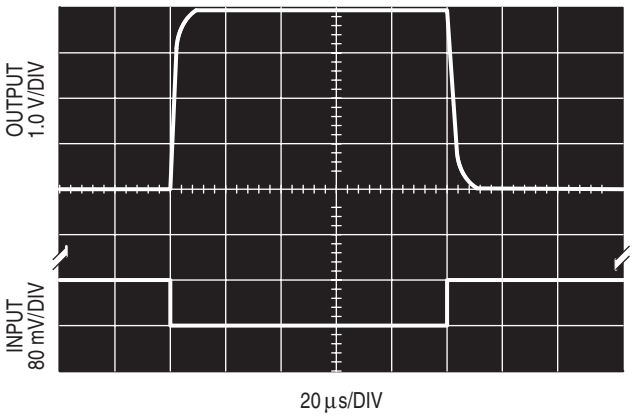


Figure 19. Large Signal Response

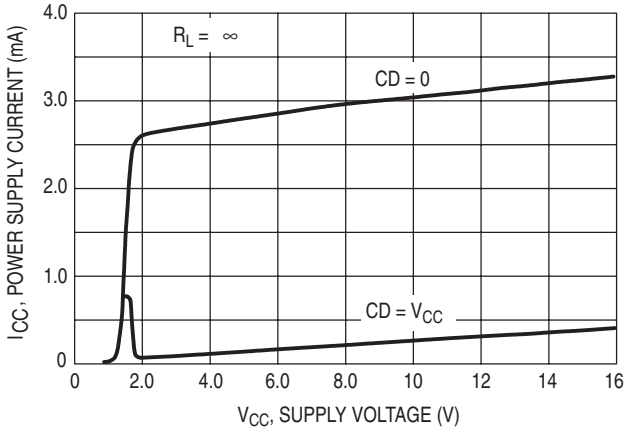


Figure 17. Power Supply Current

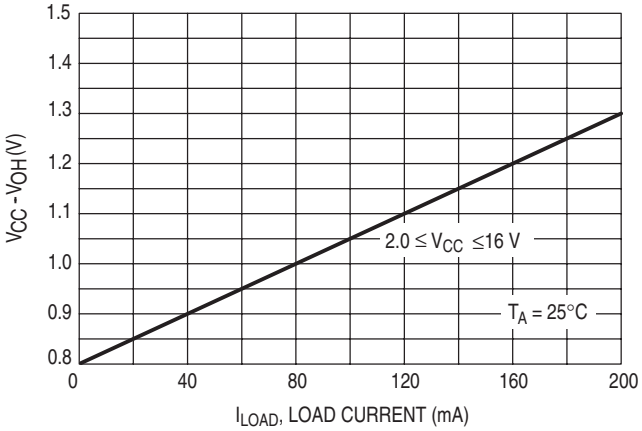


Figure 20. V_{CC}-V_{OH} @ V01, V02 versus load Current

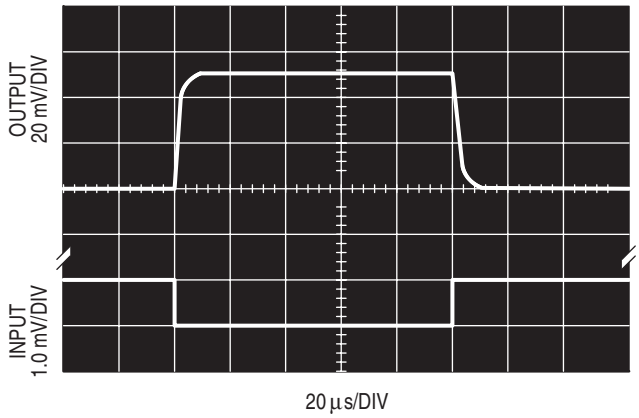


Figure 18. Small Signal Response

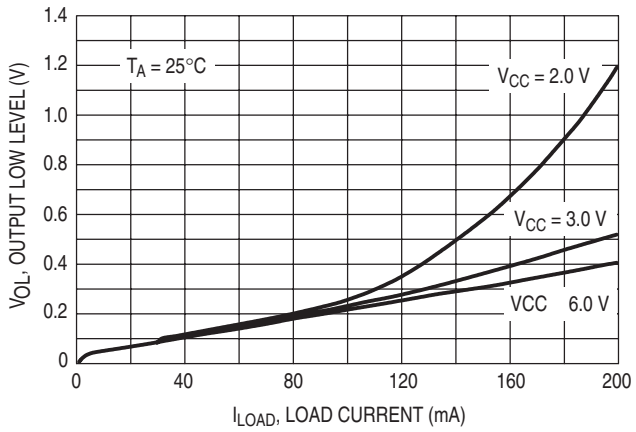


Figure 21. V_{OL} @ V01, V02 versus Load Current

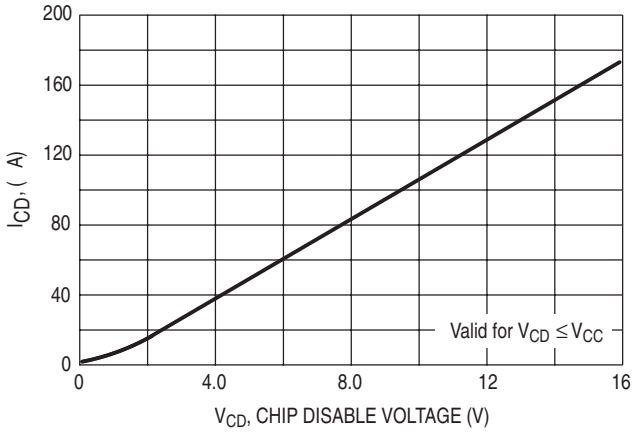
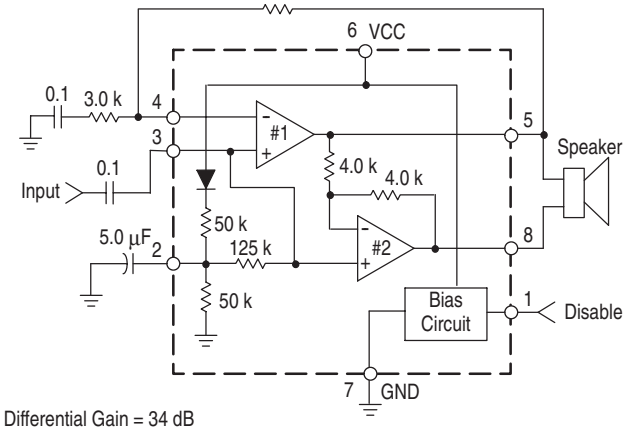


Figure 22. Input Characteristics @ CD (Pin 1)



Differential Gain = 34 dB
Frequency Response: See figure 5
Input Impedance 125 k Ω
PSRR 50 dB

Figure 23. Small Signal Response

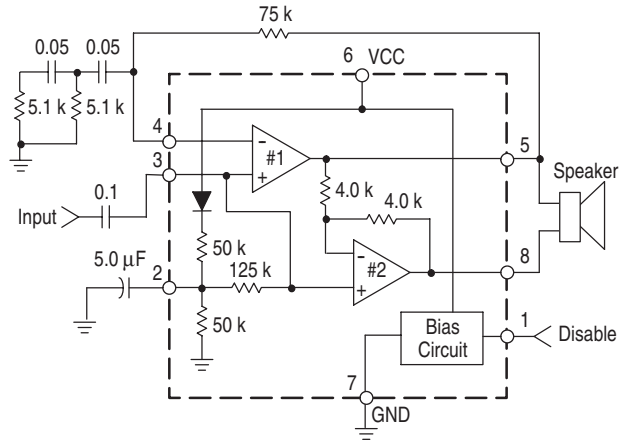


Figure 24. Audio Amplifier with Bass Suppression

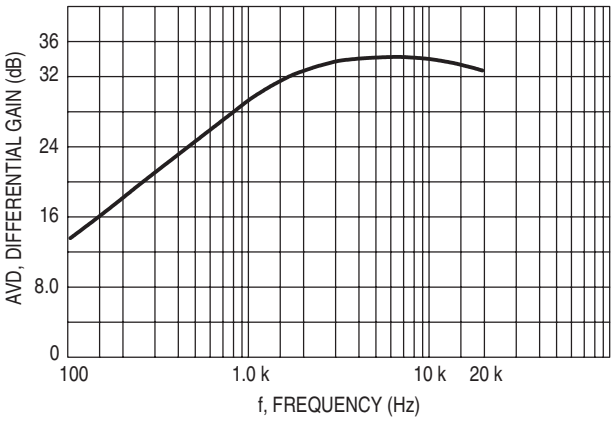


Figure 25. Frequency Response of Figure 24

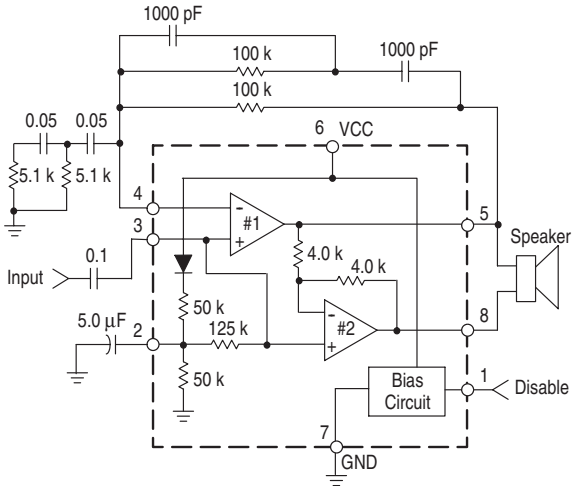


Figure 26. Audio Amplifier with Bandpass

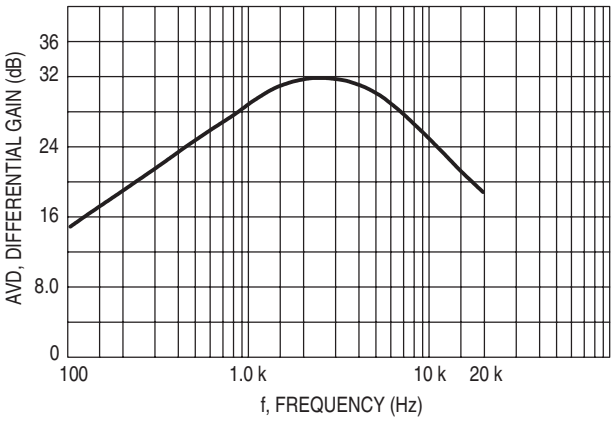
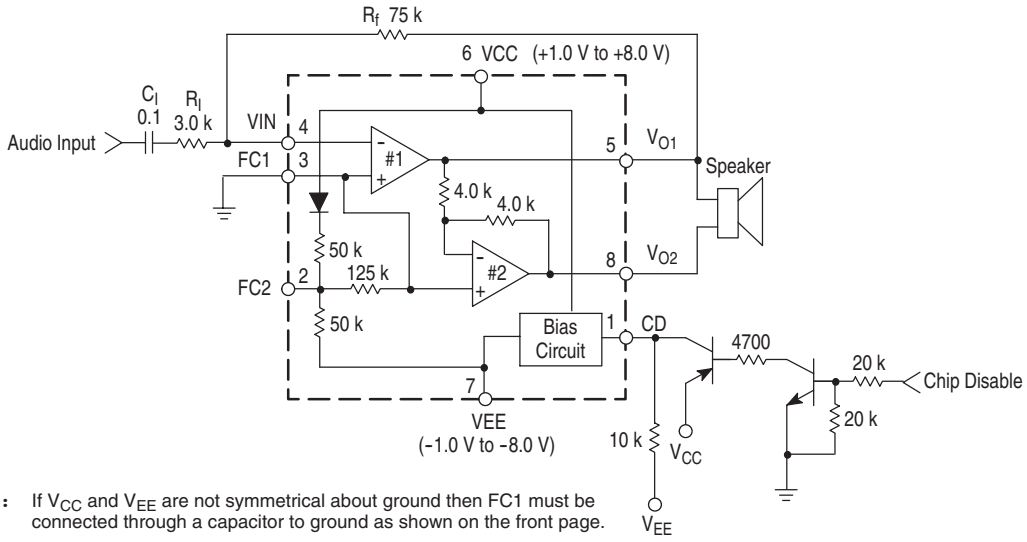


Figure 27. Frequency Response of Figure 26



NOTE: If V_{CC} and V_{EE} are not symmetrical about ground then FC1 must be connected through a capacitor to ground as shown on the front page.

Figure 28. Split Supply Operation

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 34119 is a low power audio amplifier capable of low voltage operation (V_{CC} = 2.0 V minimum), such as that encountered in line-powered speakerphones. The circuit provides a differential output (VO1-VO2) to the speaker to maximize the available voltage swing at low voltages. The differential gain is set by two external resistors. Pins FC1 and FC2 allow control of the amount of power supply and noise rejection, as well as providing alternate inputs to the amplifiers. The CD pin permits power down of the IC for muting purposes and to conserve power.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

AMPLIFIERS

Referring to the Internal Block Diagram on page 2, the internal configuration consists of two identical operational amplifiers. Amplifier #1 has an open loop gain of ≥80 dB (at f ≤ 100 Hz), and the closed loop gain is set by external resistor R_F and R_I. The amplifier is unity gain stable, and has a unity gain frequency of approximately 1.5 MHz. In order to adequately cover the telephone voice band (300 Hz to 3400 Hz), a maximum closed loop gain of 46 is recommended. Amplifier #2 is internally set to a gain of - 1.0 (0 dB).

The outputs of both amplifiers are capable of sourcing and sinking a peak current of 200 mA. The outputs can typically swing to within ≈0.4 V above ground, and to within ≈1.3 V below V_{CC}, at the maximum current. See Figures 20 and 21 for V_{OH} and V_{OL} curves.

The output dc offset voltage (V_{O1} - V_{O2}) is primarily a function of the feedback resistor (R_F), and secondarily due to the amplifiers' input offset voltages. The input offset voltage of the two amplifiers will generally be similar for a particular IC, and therefore nearly cancel each other at the outputs. Amplifier #1's bias current, however, flows out of V_{IN} (Pin 4) and through R_F, forcing V_{O1} to shift negative by an amount equal to [$R_F \cdot I_{IB}$]. V_{O2} is shifted positive an equal amount. The output offset voltage, specified in the Electrical Characteristics, is measured with the feedback resistor shown in the Typical Applications Circuit, and therefore takes into account the bias current as well as internal offset voltages of the amplifiers. The bias current is constant with respect to V_{CC}.

FC1 AND FC2

Power supply rejection is provided by the capacitors (C1 and C2 in the Typical Applications Circuit) at FC1 and FC2. C2 is somewhat dominant at low frequencies, while C1 is dominant at high frequencies, as shown in the graphs of Figures 6 to 9. The required values of C1 and C2 depend on the conditions of each application. A line powered speakerphone, for example, will require more filtering than a circuit powered by a well regulated power supply. The amount of rejection is a function of the capacitors, and the equivalent impedance looking into FC1 and FC2 (listed in the Electrical Characteristics as R_{FC1} and R_{FC2}).

In addition to providing filtering, C1 and C2 also affect the turn-on time of the circuit at power-up, since the two capacitors must charge up through the internal 50 k and 125 k. resistors. The graph of Figure 29 indicates the turn-on time upon application of V_{CC} of +6.0 V. The turn-on time is ≈60% longer for V_{CC} = 3.0 V, and ≈20% less for V_{CC} = 9.0 V. Turn-off time is <10 μs upon removal of V_{CC}.

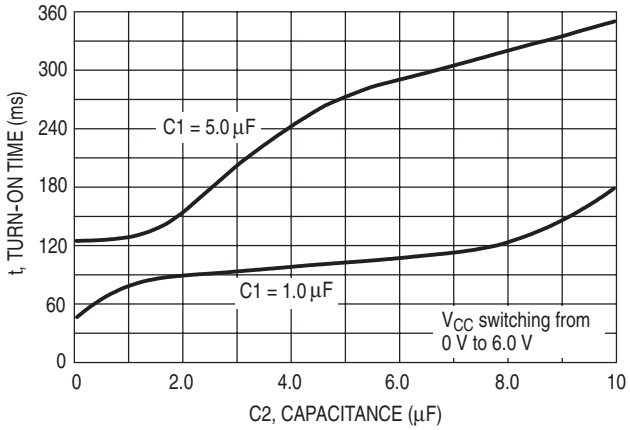


Figure 29. Turn-On Time versus C1 and C2 at Power-On

CHIP DISABLE

The Chip Disable (Pin 1) can be used to power down the IC to conserve power, or for muting, or both. When at a Logic "0" (0 V to 0.8 V), the 34119 is enabled for normal operation. When Pin 1 is at a Logic "1" (2.0 V to V_{CC} V), the IC is disabled. If Pin 1 is open, that is equivalent to a Logic "0," although good design practice dictates that an input should never be left open. Input impedance at Pin 1 is a nominal 90 kΩ. The power supply current (when disabled) is shown in Figure 17.

Muting, defined as the change in differential gain from normal operation to muted operation, is in excess of 70 dB. The turn-off time of the audio output, from the application of the CD signal, is <2.0 μs, and turn-on time is 12 ms-15 ms. Both times are independent of C1, C2, and V_{CC}.

When the 34119 is disabled, the voltages at FC1 and FC2 do not change as they are powered from V_{CC}. The outputs, VO1 and VO2, change to a high impedance condition, removing the signal from the speaker. If signals from other sources are to be applied to the outputs (while disabled), they must be within the range of V_{CC} and Ground.

POWER DISSIPATION

Figures 10 to 12 indicate the device dissipation (within the IC) for various combinations of V_{CC}, R_L, and load power.

The maximum power which can safely be dissipated within the MC34119 is found from the following equation:

$$P_D = (140°C - T_A)/\theta_{JA}$$

where T_A is the ambient temperature; and θ_{JA} is the package thermal resistance (100°C/W for the standard DIP package, and 180°C/W for the surface mount package.)

The power dissipated within the 34119, in a given application, is found from the following equation:

$$P_D = (V_{CC} \times I_{CC}) + (I_{RMS} \times V_{CC}) - (R_L \times I_{RMS}^2)$$

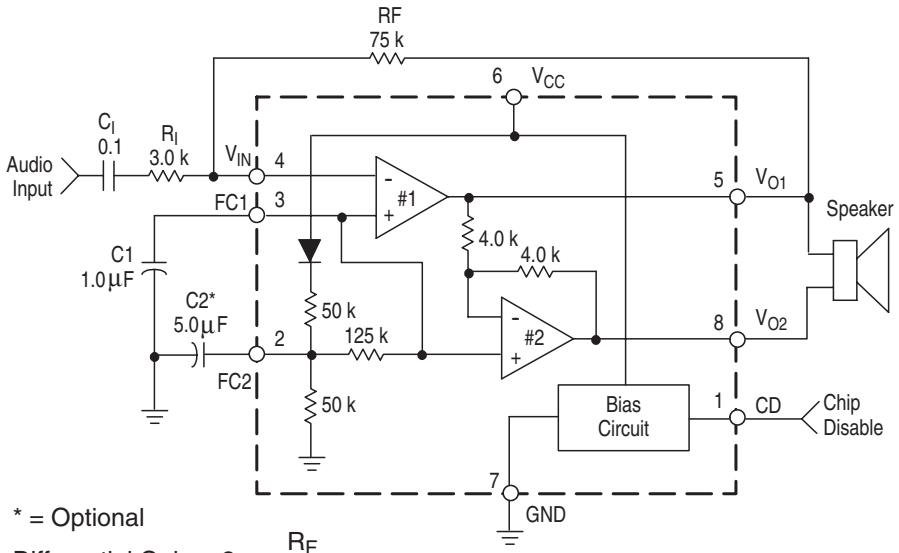
where I_{CC} is obtained from Figure 17; and I_{RMS} is the RMS current at the load; and R_L is the load resistance.

Figures 10 to 12, along with Figures 13 to 15 (distortion curves), and a peak working load current of ±200 mA, define the operating range for the 34119. The operating range is further defined in terms of allowable load power in Figure 16 for loads of 8.0Ω, 16Ω and 32Ω. The left (ascending) portion which 10% distortion occurs. The center flat portion of each curve is defined by the maximum output current capability of the 34119. The right (descending) portion of each curve is defined by the maximum internal power dissipation of the IC at 25°C. At higher ambient temperatures, the maximum load power must be reduced according to the above equations. Operating the device beyond the current and junction temperature limits will degrade long term reliability.

LAYOUT CONSIDERATIONS

Normally a snubber is not needed at the output of the 34119, unlike many other audio amplifiers. However, the PC board layout, stray capacitances, and the manner in which the speaker wires are configured, may dictate otherwise. Generally, the speaker wires should be twisted tightly, and not more than a few inches in length.

TYPICAL APPLICATIONS



* = Optional

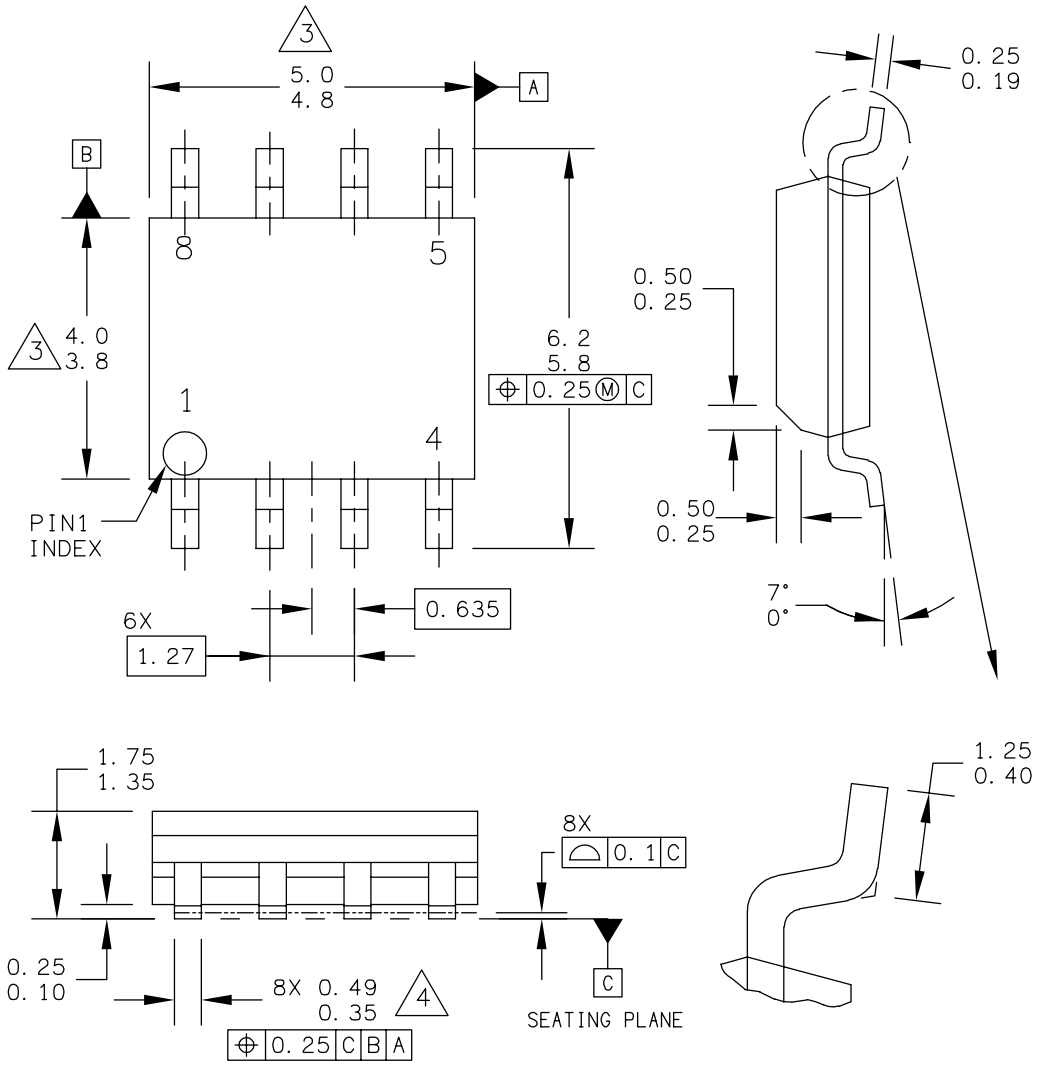
Differential Gain = $2 \times \frac{R_F}{R_I}$

This device contains 45 active transistors.

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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D SUFFIX
EF SUFFIX (PB-FREE)
PLASTIC PACKAGE
98ASB42564B
ISSUE U

34119

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
2.0	11/2006	• Converted to the current Freescale format • Implemented Revision History page • Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Maximum Ratings on page 4. Added note with instructions from www.freescale.com • Updated the Package drawing to the current revision
3.0	12/2006	• Restated note Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics. on page 4

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