MC14416
MC14418

MOS LSI
(LOW-POWER COMPLEMENTARY MOS)

TSAC
TIME SLOT ASSIGNER CIRCUITS

PER CHANNEL, ADDRESSABLE TIME SLOT ASSIGNER CIRCUITS (TSACs)

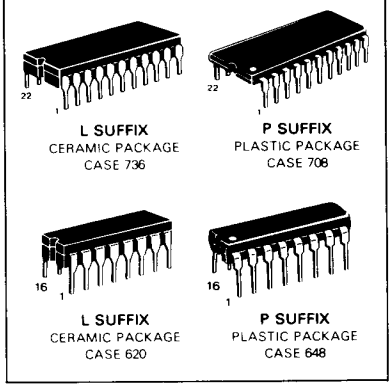
The MC14416 and MC14418 are per channel devices that allow variable codec time slot assignment to be programmed through a serial microprocessor port (0-63 time slots). Both devices have independent transmit and receive frame syncs and enables. They also include chip select and clear to send signals which simplify system design.

The MC14418 provides the additional addressing capability which allows a parallel bus back plane in the channel group. In addition, the MC14418 provides control bits which can be used for the power down, ring enable and ring trip functions on a line circuit.

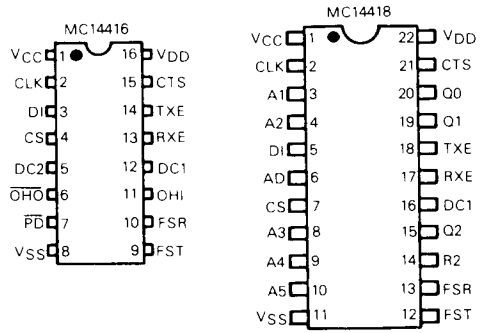
The MC14416 provides the ability to multiplex off hook signals for a bank of TSACs.

Both devices are fabricated using the CMOS technology for reliable low power performance. The MC14418 is the full featured device produced in a 22-pin package. The MC14416 without the addressing capability is offered in a 16-pin package.

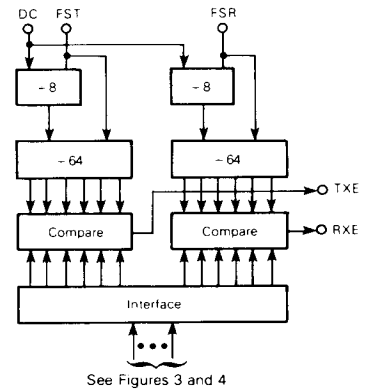
- Low Power
- 5-Volt Interface on Microprocessor Port
- 5-16 Volt Output Logic Levels
- Independent Transmit and Receive Frame Syncs and Enables
- Up to 64 Time Slots Per Frame
- For Use With Up to 2.56 MHz Clocks
- Provides Power Down Control for Line Circuits
- Compatible with MC14400/01/02/03/05 and MK5116 Codecs
- Provides the Ring Enable and Ring Trip Functions (MC14418)
- Allows Use of a Parallel Backplane for Line Circuits Due to the Hard Wired Address Feature (MC14418)
- Off-Hook Multiplex Control (MC14416)
- CMOS Metal Gate for High Reliability



PIN ASSIGNMENTS



BLOCK DIAGRAM



See Figures 3 and 4

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Level Shift Voltage	V_{CC}	−0.5 to V_{DD}	Vdc
Input Voltage Inputs Referenced to V_{DD} to V_{CC}	V_{in1} V_{in2}	−0.5 to V_{DD} +0.5 −0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +165	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$)

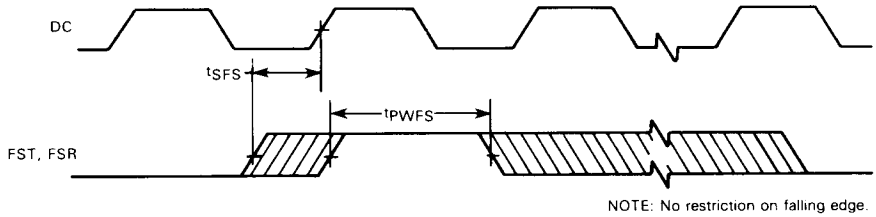
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
DC Supply Voltage $V_{SS} = 0$ V	V_{DD}	–	4.5	12	16	V
DC Supply Voltage $V_{SS} = 0$ V	V_{CC}	–	4.5	5	V_{DD}	V
Output Current TXE, RXE, Q0, Q1, Q2, $\overline{P_D}$						
($V_{OL} = 0.4$ V)	I_{OL}	5	0.51	–	–	mAdc
($V_{OL} = 1.0$ V)		12	2.0	4.0	–	
($V_{OH} = 4.6$ V)	I_{OH}	5	−0.20	–	–	mAdc
($V_{OH} = 1.0$ V)		12	−2.0	−4.0	–	
Output Current CTS, OHO						
($V_{OL} = 0.8$ V)	I_{OL}	5	3.0	5.5	–	mAdc
($V_{OL} = 0.8$ V)		12	6.6	11.5	–	
($V_{OL} = 1.5$ V)		12	12.0	20.0	–	
($V_{OH} = 0.8$ V)	I_{OH}	5	−8	−20	−40	µAdc
($V_{OH} = 2.0$ V)		5	−6	−18	−40	
($V_{OH} = 0.8$ V)		12	−40	−100	−200	
($V_{OH} = 2.0$ V)		12	−35	−90	−200	
($V_{OH} = 10.5$ V)		12	−15	−30	−60	
Input Voltage (CMOS) "0" Level FST, FSR, R2, DC1, DC2, A1, A2	V_{IL}	5 12	– –	– –	1.0 2.4	Vdc
A3, A4, A5, OHI "1" Level	V_{IH}	5 12	4.0 9.6	– –	– –	Vdc
Input Current OHI (Active Pull Down)	I_{inH}	5 12	+1.5 +10	+4.0 +25	+15 +100	µAdc
Input Voltage (TTL) "0" Level CLK, CS, AD, DI	V_{IL}	5 12	– –	– –	0.8 0.8	Vdc
$V_{CC} = 5$ V "1" Level	V_{IH}	5 12	2.00 2.00	– –	– –	Vdc
Input Current	I_{in}	15	–	$\pm 10^{-5}$	±0.1	µAdc
Input Capacitance	C_{in}	–	–	5	7.5	pF
Total Supply Current (Outputs Unloaded) $V_{DD} = 12$ V DC1 at 2.048 MHz $V_{DD} = 5$ V	I_T	12 5	– –	3 2	6 4	mAdc
Total Supply Current (Power Down) MC14418 Only After CTS = V_{DD} CLK, CS, AD, DI Inputs ≤ 0.6 V	I_{PD}	–	–	–	0.1	mAdc

SWITCHING CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25°C$, unless otherwise noted)

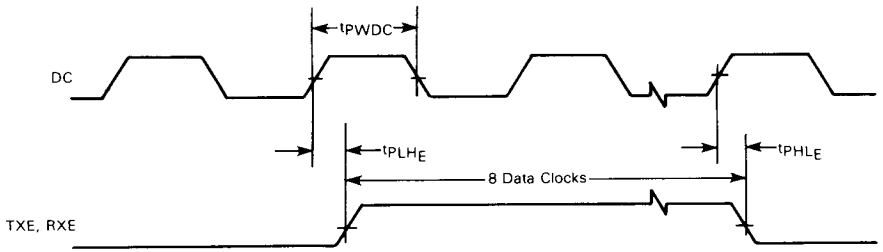
Characteristic	Symbol	Fig.	V_{DD}	Min	Typ	Max	Unit
Output Rise Time TXE, RXE, Q0, Q1, Q2, $\overline{P_D}$	t_r	–	5 12	– –	100 50	200 100	ns
Output Fall Time TXE, RXE, Q0, Q1, Q2, $\overline{P_D}$	t_f	–	5 12	– –	100 50	200 100	ns
Frame Sync Setup Time	t_{SFS}	1	5 12	−150 −75	– –	+150 +75	ns
Frame Sync Pulse Width	t_{PWFS}	1	5 12	200 100	– –	– –	ns
Propagation Delay — DC to TXE, RXE (Note 1) $C_L = 20$ pF	t_{PLHE}, t_{PHLE}	1	5 12	– –	130 80	180 125	ns
Data Clock Frequency	f_{DC}	–	5 12	– –	– –	2.048 2.6	MHz
Data Clock Pulse Width (at $f_{DC(MAX)}$)	t_{PWDC}	1	5 12	200 140	244 192	293 260	ns
Clock Frequency	f_{CLK}	–	5 12	00 00	– –	0.3 0.3	MHz
Clock Pulse Width (at $f_{CLK(MAX)}$)	t_{PWC}	2	5 12	0.5 0.5	– –	– –	µs
Address and Data Setup Time	t_{su}	2	5 12	300 300	– –	– –	ns
Address and Data Hold Time	t_h	2	5 12	200 200	– –	– –	ns
Propagation Delay — DC1 to CTS	t_{PCL}	2	5 12	– –	– –	250 150	ns
DC1 or FST to CTS 10K Pullup or Equivalent	t_{PCH}	2	5 12	– –	– –	300 200	ns
Propagation Delay — DC to PD	t_{PQ}	2	5 12	– –	– –	300 200	ns
DC to Q0-Q2	t_{PQ}	2	5 12	– –	– –	300 200	ns
Propagation Delay — R to Q2	t_P	2	5 12	– –	100 50	200 100	ns
Chip Select Setup Time Leading CS to Falling CLK	t_{SCS}	2	5 12	1 1	–	–	µs
Chip Select Hold Time Falling CTS to Falling CS	t_{HCS}	2	5 12	10 10	– –	– –	ns

NOTE 1: For time slot 0, t_{PHLE} and t_{PLHE} are measured from leading edge of DC or FST (FSR), whichever occurs last.

FIGURE 1 — TIMING DIAGRAMS



NOTE: No restriction on falling edge.



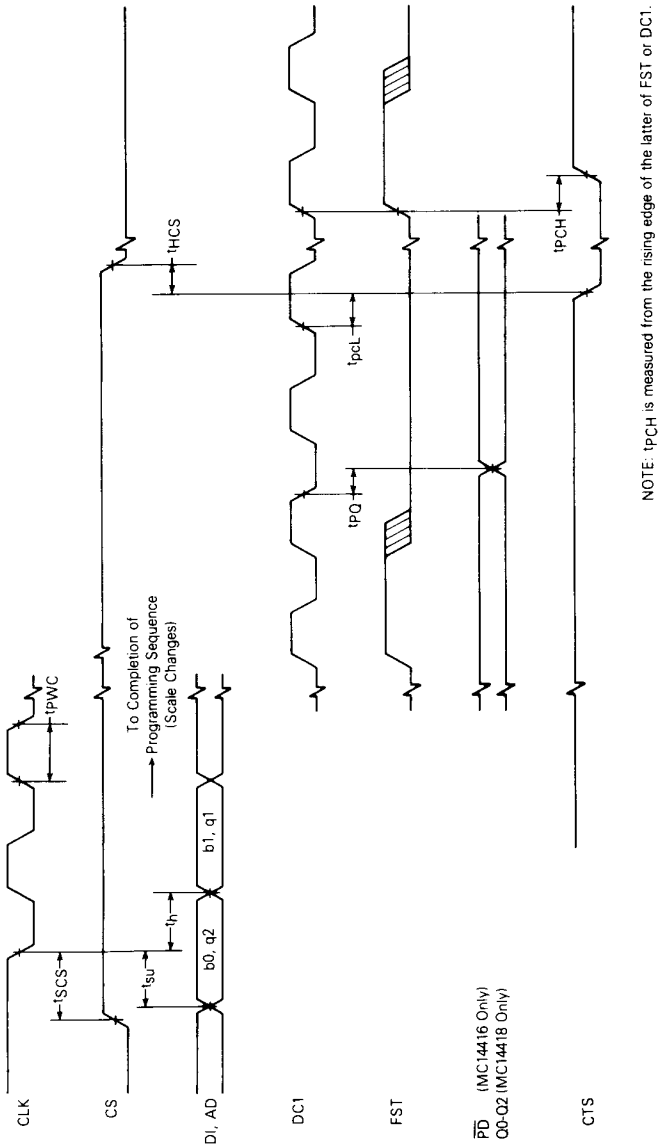


FIGURE 2 – PROPAGATION DELAYS FOR PROCESSOR INTERFACE PINS

NOTE: t_{PCH} is measured from the rising edge of the latter of FST or DC1.

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FIGURE 3 — MC14418 22 PIN

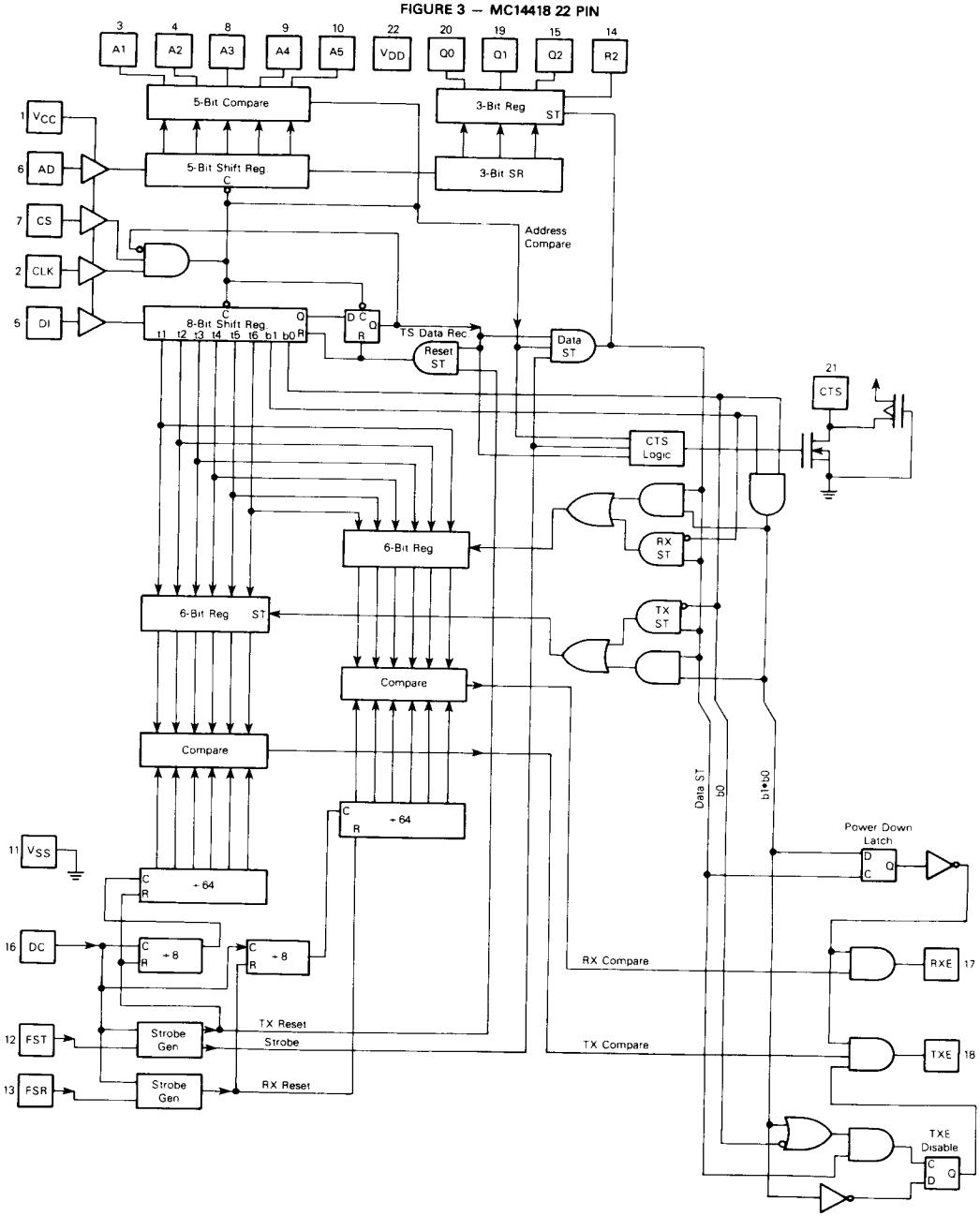
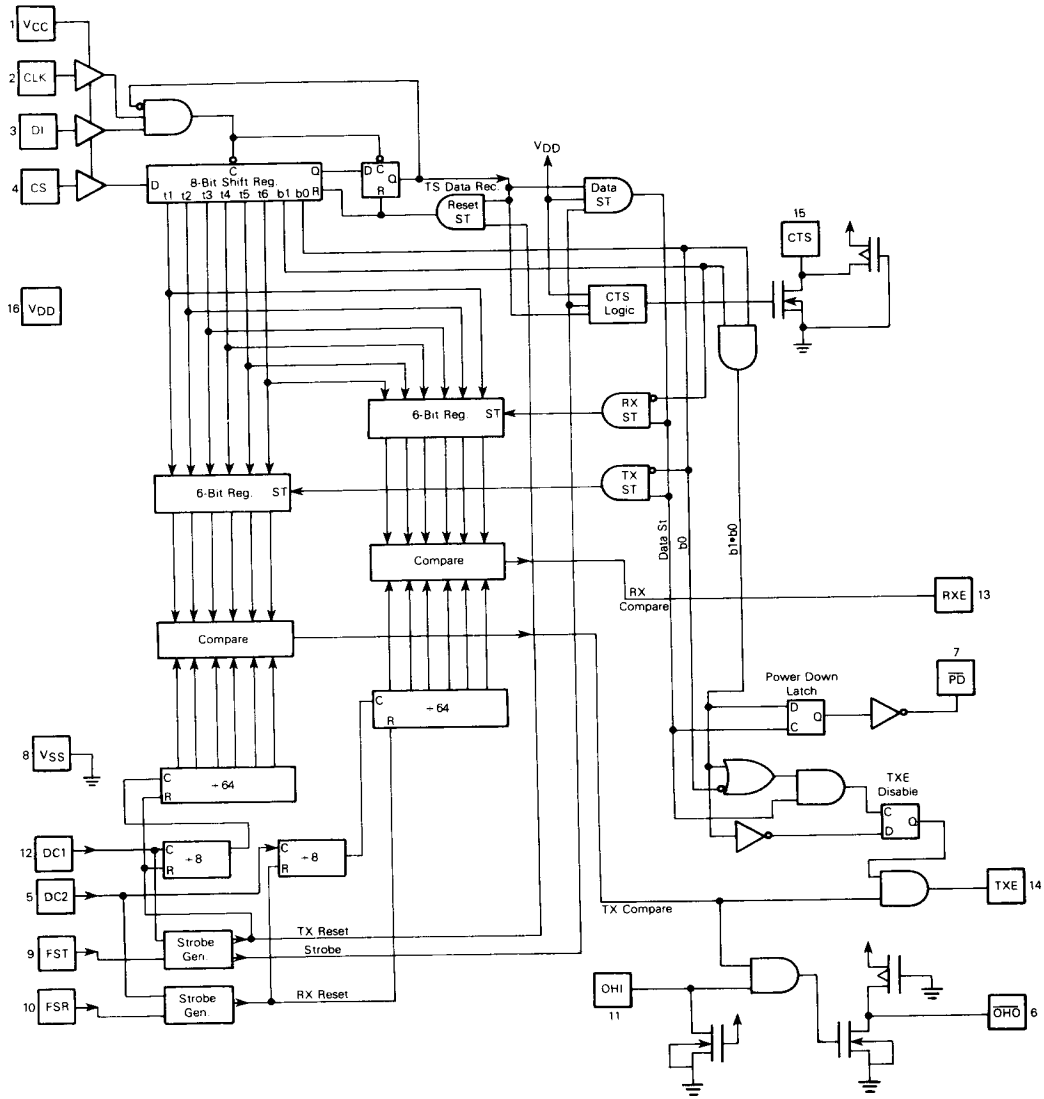


FIGURE 4 — MC14416 16 PIN



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GENERAL DEVICE DESCRIPTION

The MC14416 and MC14418 TSACs are microprocessor peripherals intended to be used to control and supervise per channel codec subscriber channel units. The TSACs consist of three basic functions.

The Serially Programmable Microprocessor Port consists of V_{CC}, CLK, DI, CS and CTS for the MC14416 and further includes AD and A1 through A5 for the MC14418. This port allows the call processing microprocessor to access load data into each TSAC. See the applications section for a detailed description of the microprocessor port. Figure 5 defines the data word bit assignments.

The Supervision Controls consist of Q0, Q1, Q2, R2 on the MC14418 and OHI, $\overline{OHO}$ and $\overline{PD}$ on the MC14416. These functions provide data path for the supervision and control of user selected requirements in the subscriber channel unit. Figure 3 shows some typical uses of these bits.

The Time Slot Computation section of the chip derives separate transmit and receive time slot outputs (TXE and RXE) for the controlled codec from the bit rate clock and sync pins DC1, DC2, FST and FSR, respectively. The computed time slot is then derived from the information received through the microprocessor port.

PIN DESCRIPTIONS

V_{CC} (Positive Supply for Microprocessor Port) — If this is a 5-volt supply, AD, DI, CS and CLK are TTL compatible CMOS inputs. V_{CC} may be any voltage from 4.5 V to V_{DD} allowing either TTL or CMOS compatibility.

CS (Chip Select Input) — For the MC14418, the pin is used to select a bank of TSACs.

For the MC14416, the CS is used to select that individual TSAC. All CSs are normally held low. To PROGRAM A SPECIFIC TSAC, CS must go high prior to the first falling edge of CLK. CS must stay high until the selected CTS goes low to guarantee a valid access.

CS is synchronous with DI, AD and CLK. CS can be asynchronous with DC1, DC2, FST or FSR. (This pin is normally intended to be set by a microprocessor.)

CLK (Microprocessor Clock Input) — Serial data is entered through the AD and DI pins under the control of CLK. The data is entered on the trailing edge of CLK. CLK is synchronous with CS, AD and DI and can be asynchronous with the TSAC's data clocks (DC1 or DC2).

DI (Serial Time Slot Data and Mode Input) — 8-bit words are clocked into the device through DI under the control of CLK after CS is brought high. The first 2 bits of DI control the various programming modes while the last 6 bits are time slot data. (See Figure 5 for the format of the DI word.)

AD (Serial Address and Control Bits Input — MC14418 only) — 8-bit words are clocked into the device through AD under the control of CLK after CS is brought high. AD words are loaded in parallel with the DI words. The first 3 bits of AD program the control bits Q0, Q1, and Q2 while the last 5 bits are compared with the hardware address on A1 through A5 to identify a specific TSAC in a bank. (See Figure 5 for the format of the AD words.)

A1-A5 (Codec Address Inputs — MC14418 only) — These five pins provide a unique identity for each TSAC. The TSAC address pins are either hardwired on the PC board or in the channel bank backplane. The processor loads the 5-bit address data into AD, and each MC14418 in the selected bank compares this data to the hardwired address set by its A1-A5 to determine if the time slot data loaded into DI is intended for that TSAC. By this process, only one of 32 TSACs in a bank will accept the transmitted time slot data. A1-A5 are CMOS inputs, logical "1" = V_{DD} and logical "0" = V_{SS}.

Q0, Q1, Q2 (Status Bit Outputs — MC14418 Only) — These three bits are programmed by the first 3 bits of the 8-bit word which is loaded into AD. The bits are used for the basic control functions of a line circuit. See the applications section (ref. Figure 11) for an example of how these status bits are used. In this example, Q1 selects to receive data streams, Q0 is used for the power down control, and Q2 is used for the ring enable. These are CMOS outputs.

R2 (Reset Input for Q2) — The R2 input provides a direct reset of the Q2 output. When R2 is taken high, Q2 is set to "0" independent of all other TSAC functions. See the applications section (ref Figure 11) for an example of how this reset bit is used, i.e., the ring trip signal is used to reset Q2 which is the ring enable. This combination of R2 and Q2 allows a simple solution to the ring trip function.

CTS (Clear to Send Output) — This output provides a simple diagnostic capability for the processor TSAC combination. The selected TSAC outputs the CTS signal after it has accepted data. This output goes low three data clock cycles after the next FST, and returns high on the subsequent FST. For the MC14418, only the TSAC which accepts transmitted data will respond with CTS low. All other TSACs in the bank will leave CTS high. The CTS output is an open drain transistor with a weak internal pullup. Normally a bank of CTS outputs are wire ORed together to provide a single diagnostic bus, which can be used to verify that transmitted data was properly acknowledged by some TSAC in the bank.

CTS may also be used to strobe additional supervision data into a selected channel unit, due to its dependence upon the address selection logic of the MC14418.

DC1, DC2 (Data Clock Input) — The data clock input establishes the bit rate of the TSAC and its associated codec. It is intended to be between 1.536 and 2.56 MHz and is the same as the codec's bit rate clock. Both TSACs divide

these inputs by eight to derive the time slot rate. For the MC14418, DC1 provides the data rate clock for both transmit and receive time slot computation. The MC14416 derives transmit timing from DC1 and receive timing from DC2. They are CMOS compatible inputs.

FST, FSR (Frame Sync Transmit and Frame Sync Receive Inputs) — These inputs are leading-edge sensitive synchronization pulses for establishing the position of time slot zero in the transmit and receive frames, respectively.

The rising edge of DC (1 or 2) associated with the rising edge of FST or FSR identifies the sign bit period of time slot zero. See Figures 6 and 7 for detailed timing. In the MC14418, both zero time slots are derived from DC1 but may be different by an integral number of bits. In the MC14416, FST and DC1 derive the transmit time slot zero, while FSR and DC2 derive the receive time slot zero independently. DC1 and DC2 can be asynchronous. FSR and FST are CMOS inputs.

TXE, RXE (Transmit Enable and Receive Enable Outputs) — These are the outputs of the time slot computation circuitry. Each output is high for eight data clocks; i.e., an integral number of time slots after the rising edge of FST and FSR for TXE and RXE, respectively. The binary number entered in the last 6 bits of the DI input indicates the number of eight data clock intervals (time slots) between FST or FSR and the eight data clock time slot, when TXE or RXE will be high. These are CMOS B series outputs which will drive one TTL LS input when V_{DD} is five volts. See Figure 6 and Figure 7 for detailed timing and numbering.

TABLE 1 — BASIC OPERATION OF MC14418

Input Conditions				Action to Outputs After Next FST						
TS Data Received	Address Compare	b0	b1	CTS	TX Reg. Load	RX Reg. Load	TXE Disabled	RXE Disabled	Data Reg. (Q0-Q2) Load	Time Slot Counters Running
No	X	X	X	1	No	No	No Change	No Change	No	No Change
Yes	No	X	X	1	No	No	No Change	No Change	No	No Change
Yes	Yes	0	0	0	Yes	Yes	No	No	Yes	Yes
Yes	Yes	0	1	0	Yes	No	No	No	Yes	Yes
Yes	Yes	1	0	0	No	Yes	No Change	No	Yes	Yes
Yes	Yes	1	1	0	X	Yes	Yes	Yes	Yes	No

TABLE 2 — BASIC OPERATION OF MC14416

Input Conditions					Action to Outputs After Next FST			
TX Data Received	CS	b0	b1	CTS	TX Reg. Load	RX Reg. Load	TXE Disabled	$\overline{PD}$ Output
No	X	X	X	1	No	No	No Change	No Change
Yes	0	X	X	1	No	No	No Change	No Change
Yes	1	0	0	0	Yes	Yes	No	1
Yes	1	0	1	0	Yes	No	No	1
Yes	1	1	0	0	No	Yes	No Change	1
Yes	1	1	1	0	No	No	Yes	0

Note 1: The $\overline{OHO}$ output remains operational when TXE is disabled.

FIGURE 5 – FORMAT FOR DI AND AD WORDS

MC14418	DI Word Input First Bit Sent								AD Word Input First Bit Sent							
Results of Bit Pattern	Mode		Time Slot Data						Status Bits			Address Data				
	b0	b1	t6	t5	t4	t3	t2	t1	q2	q1	q0	a5	a4	a3	a2	a1
Assign TSAC 16 to the first time slot (TSO) for both receive and transmit and set its status bit to 011	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0
Assign TSAC 1 to time slot 8 for receive only and set status bits to 011	1	0	0	0	1	0	0	0	0	1	1	0	0	0	0	1
Assign TSAC 8 to time slot 2 for transmit only and set status bits to 011	0	1	0	0	0	0	1	0	0	1	1	0	1	0	0	0
Program TSAC 4 to idle (no time slot outputs) and set status bits to 011	1	1	X	X	X	X	X	X	0	1	1	0	0	1	0	0
Codec 1 is powered down (80 = 0)	X	X	X	X	X	X	X	X	0	1	0	0	0	0	0	1
Line circuit associated with codec 2 is programmed to ring the line (See Fig. 13)	X	X	X	X	X	X	X	X	1	1	1	0	0	0	1	0

MC14416								
Assign the selected TSAC to the first time slot (TSO) for both receive and transmit and set $\overline{PD} = 1$	0	0	0	0	0	0	0	0
Assign the selected TSAC to time slot 8 for receive only and set $\overline{PD} = 1$	1	0	0	0	1	0	0	0
Assign the selected TSAC to time slot 2 for transmit only and set $\overline{PD} = 1$	0	1	0	0	0	0	1	0
Power down the selected TSAC, i.e., $\overline{PD}$ to "0"	1	1	X	X	X	X	X	X

*See Figures 12 and 13 for the hardware implementations using MC14418 and MC14416.

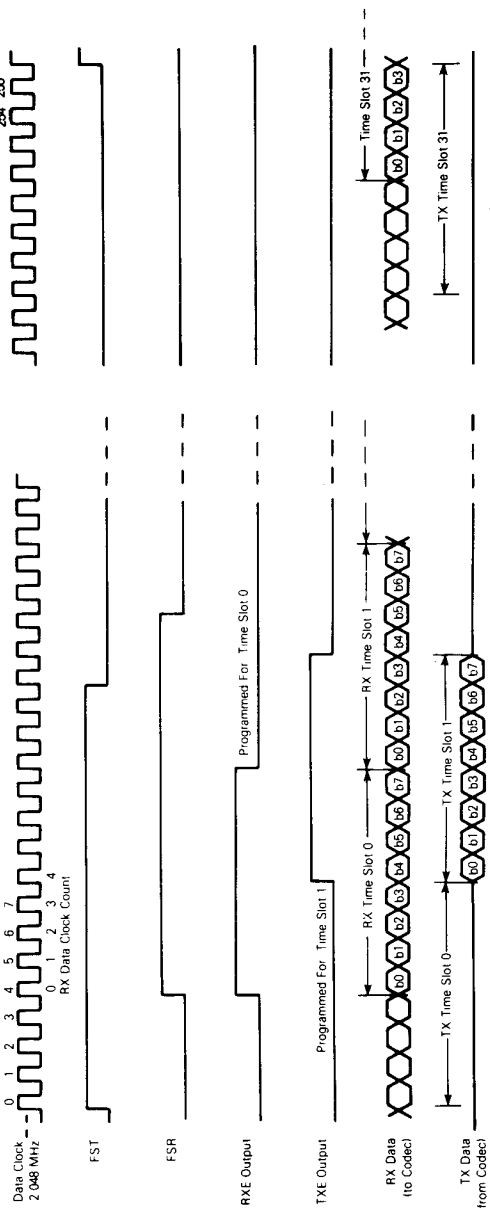

FIGURE 6 – DATA MULTIPLEX TIMING FOR 2.048 MHz

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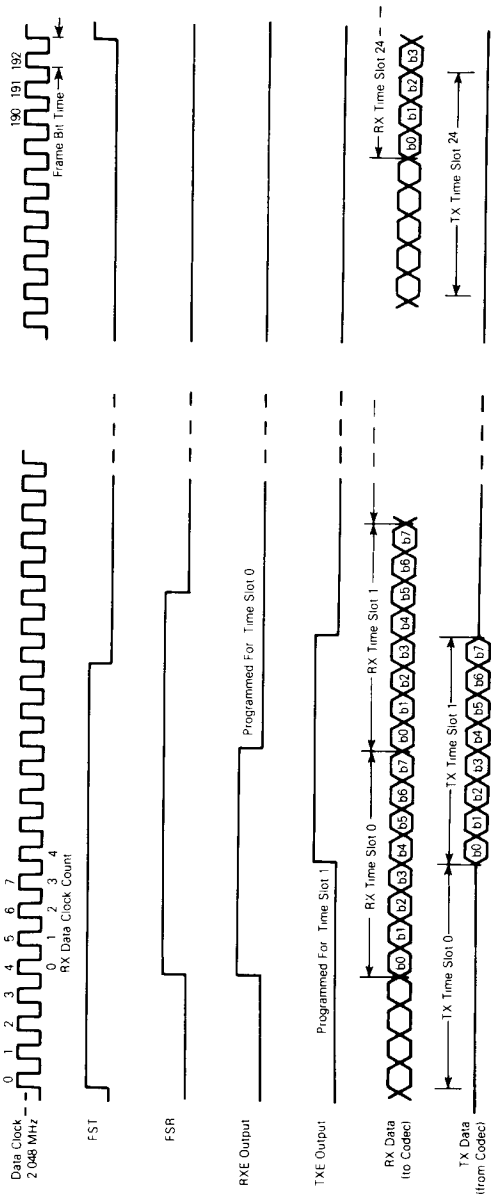


FIGURE 7 – DATA MULTIPLEX TIMING FOR 1.544 MHz

$\overline{PD}$ (Power Down Output — MC14416 Only) — The $\overline{PD}$ output is normally high. It is set high whenever b0 or b1 is a zero and the TSAC is programmed. If b0 and b1 are both one, then PD will be set low. This output is intended to be used to power down other circuitry in the channel unit when the channel unit is idle. This is a CMOS B series output which will drive one TTL LS load when V_{DD} is five volts.

OHI (Off Hook Input — MC14416 Only) — The OHI is a CMOS input with an internal pull-down resistor. A DC level at this pin will appear at the OHO output during the programmed TXE time slot.

$\overline{OHO}$ (Off Hook Output Inverted — MC14416 Only) — During the programmed transmit time slot, the data at OHI appears inverted at $\overline{OHO}$; otherwise $\overline{OHO}$ will be pulled high passively. The $\overline{OHO}$ output is an open drain N-channel transistor with a weak pull-up to V_{DD}. A number of these outputs can be wire ORed together to form a hook status bus consisting of a serial stream of hook information from a bank of channels. When the MC14416 powers down its codec, the TXE output is disabled; but the $\overline{OHO}$ output continues to multiplex out OHI and transmit time slot information during the previously entered transmit time slot.

V_{SS} — This is the most negative supply pin and digital ground for the package.

V_{DD} — This is the most positive supply. V_{DD} is typically 12 V with an operation range of 5 to 16 volts. All logic outputs swing the full supply voltage.

APPLICATIONS

The following section is intended to facilitate device understanding through several application examples. Included are Data Multiplex Timing Diagrams, a description of the TSAC Microprocessor port, a sample program, two circuit configurations using Motorola's devices, a systems drawing and two suggested clock circuits for obtaining codec data and control clocks.

In Figures 6 and 7 are shown Data Multiplex Timing Diagrams for 2.048 MHz and 1.544 MHz data clocks. The major points to be seen from these examples are:

1) Receive and transmit programming for the MC14418 are bit synchronous and word asynchronous. The MC14416 can be completely asynchronous.
2) The rising edges of FST and FSR initiate the programming frame for transmit and receive channels, respectively, and identify transmit and receive time slot "0," respectively.
3) Time slots identify eight data clock words. In this example: the transmit time slot is programmed as time slot "1." Therefore, bits 8 through 15 after FST are time slot "1."
4) For the 1.544 MHz clock, the framing bit is at the very end of the frame.

TSAC Microprocessor Port (MC14418 and MC14416) — The MC14418 provides four pins with 5-volt microprocessor input characteristics. These are AD, CS, CLK, and DI. The input supply for these inputs is V_{CC}. The CTS output is an open drain device with a weak pull up to V_{DD}. Typically, these five pins are bused in parallel to 24 or 32 TSACs per processor port. If desired, AD, CLK, DI, and CTS may be bused to greater than 32 TSACs by using the CS input as a group select. A microprocessor port of eight bits can thus control four groups of 32 TSACs with no additional decoding, as shown in Figure 8.

In order to program any given codec to a transmit or receive time slot, the processor simply exercises the corresponding 8-bit port.

Beginning with CS1 to CS4 low, all TSACs in the bank have their data registers in the Ready for Data Mode. The microprocessor takes the appropriate CS high and clocks in two bits of data into the 32 selected TSACs through DI and AD using CLK. The microprocessor presents data on the leading edge of CLK and the TSACs clock in data on the trailing edge of CLK. After eight CLK pulses (high, then low) the 32 selected TSACs will have two new 8-bit words; one in the data register through DI and one in the address register through AD. The unique TSAC, whose last 5 bits of the address register match its hardwired address on A1 through A5, acknowledges the new data. After the next FST, the selected TSAC will pull CTS low. This event notifies the processor that its transmission has been recognized. If CTS occurs at any other time, the processor can recognize the fault condition and restart the transmission using the reset function of the TSAC chip select. The uniquely selected TSAC will load its new program data into the appropriate TIME SLOT register on the next leading edge of FST. The bank of 32 TSACs will internally reset to the Ready for Data Mode when the transmission is completed, after the next FST. The TSAC, which was uniquely selected, and which has CTS low, will clear CTS to the pulled-up condition with the next FST. The processor may now program a new time slot immediately, with or without returning the selected CS low. Time Slot data can thus be sent at the rate of once every 256 μsec. for 8 kHz sampling (FST). The processor need not operate in an interrupt mode even though the TSAC's DC and CLK are asynchronous.

The processor port of the MC14416 works similarly to the MC14418, but will accept data if CS is high, and does not compare a hardwired address to the address word.

Figure 11 shows the typical signal timing for programming the microprocessor port.

To demonstrate the programming of the TSAC, consider the following configuration. A microprocessor is used to control four groups of thirty-two TSACs through an eight-bit PIA port. Four of the PIA lines are used for group select lines. The other four lines are dedicated to CLK, DI, AD, and CTS. The TSACs are programmed by serially loading bits into the DI and AD leads. Data bits are latched on the falling edge of CLK. The PIA port is connected as shown in Figure 9. The flow chart in Figure 10 and the following program illustrate one method of TSAC programming.

Before running the following program, the address, time slot, and group number must be entered in appropriate locations. During execution, CS (group select), AD, and DI words are arranged for serial presentation to the TSACs. The bits are presented with CLK high and are latched in with the falling edge of CLK. After eight passes through the loop, the TSAC is programmed, and CTS falls on the third data clock pulse after the next FST. The program waits for CTS to go high again before removing CS to prevent aborting the TSAC's programming. This program allows a maximum rate of programming equal to one TSAC per two frames.

FIGURE 8 — TYPICAL 8-BIT PORT

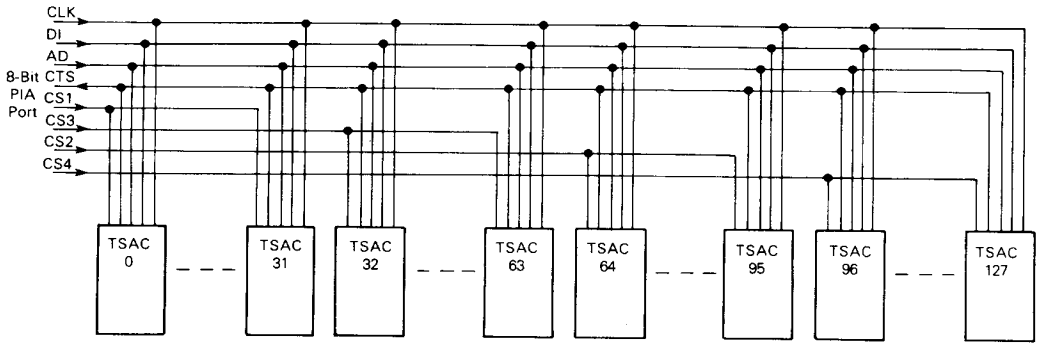


FIGURE 9 — PIA PORT ASSIGNMENT

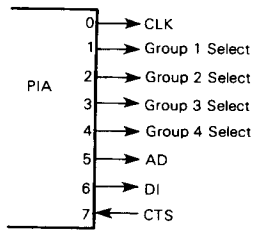
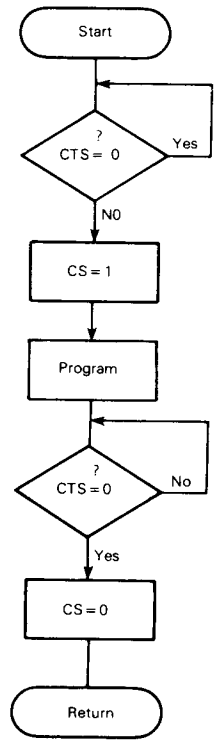


FIGURE 10 — TSAC PROGRAMMING FLOW CHART



Instructions for use:
Load in AD word (Q2, Q1, Q0, A5, A4, A3, A2, A1)
DI word (b0, b1, t6, t5, t4, t3, t2, t1)
group word
Start routine.

```
        LDAA GROUP      STORE GROUP # IN ACCA
        DECA            CHECK IF EQ. TO ONE
        BNE ONE         IF NOT GO TO NEXT TEST
        LDAB #03        EQUALS ONE
        STAB SELECT     LOAD PROPER SELECT BITS IN SELECT WORD
        BRA START       JUMP TO NEXT PART
ONE     DECA            IS GROUP EQ. TO TWO?
        BNE TWO         IF NOT GO TO NEXT TEST
        LDAB #05        LOAD PROPER SELECT BITS IN SELECT WORD
        STAB SELECT
        BRA START       JUMP TO NEXT PART
TWO     DECA            CHECK IF EQ. TO THREE
        BNE THREE       IF NOT IS EQ. TO FOUR
        LDAB #09        LOAD PROPER SELECT BITS IN SELECT WORD
        STAB SELECT
        BRA START       JUMP TO NEXT PART
THREE   LDAB #11        LOAD GROUP SELECT BITS FOR GROUP FOUR
        STAB SELECT
START   LDAA #00        INITIALIZE PIA
        STAA CONTRLB    INITIALIZE PIA
        LDAA #7F        INITIALIZE PIA
        STAA DDRB       INITIALIZE PIA
        LDAA #04        INITIALIZE PIA
        STAA CONTRLB    INITIALIZE PIA
        LDAB #80        TEST FOR CTS HIGH
WAIT    BITB PIAOUT     WAIT FOR CTS HIGH
        BEQ WAIT
        LDAA #01        NOW CTS IS HIGH, SET CLK HI AND LEAVE CS LOW
        STAA PIAOUT
        LDAA #08        INITIALIZE LAP COUNTER
        STAA COUNTER
        LDX 00          MOVE AD AND DI INPUTS
        STX 02          TO SHIFT LOCATIONS
        LDAA SELECT     BRING CS HIGH
        STAA PIAOUT
LOOP    LDAA SELECT     START BIT STUFFING
        ROL 0002        CHECK AD WORD
        BCC 02          CHECK AD WORD
        ORAA 20         CHECK AD WORD
        ROL 0003        CHECK DI WORD
        BCC 02          CHECK DI WORD
        ORAA 40         CHECK DI WORD
        STAA PIAOUT     WRITE BITS TO TSAC
        DECA            WRITE FALLING EDGE OF CLK
        NOP             WRITE FALLING EDGE OF CLK
        NOP             WRITE FALLING EDGE OF CLK
        STAA PIAOUT     WRITE FALLING EDGE OF CLK
        DEC COUNTER     DECREMENT LAP COUNTER
        BNE LOOP        TEST FOR LOOP COMPLETION
        LDAB #80        TEST AND WAIT FOR CTS LOW
ISITLO  BITB PIAOUT     TEST AND WAIT FOR CTS LOW
        BNE ISITLO      TEST AND WAIT FOR CTS LOW
        CLR PIAOUT      REMOVE CS (GROUP SELECT)
        RTS             RETURN FROM SUBROUTINE
```

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FIGURE 11 – MICROPROCESSOR PORT TIMING

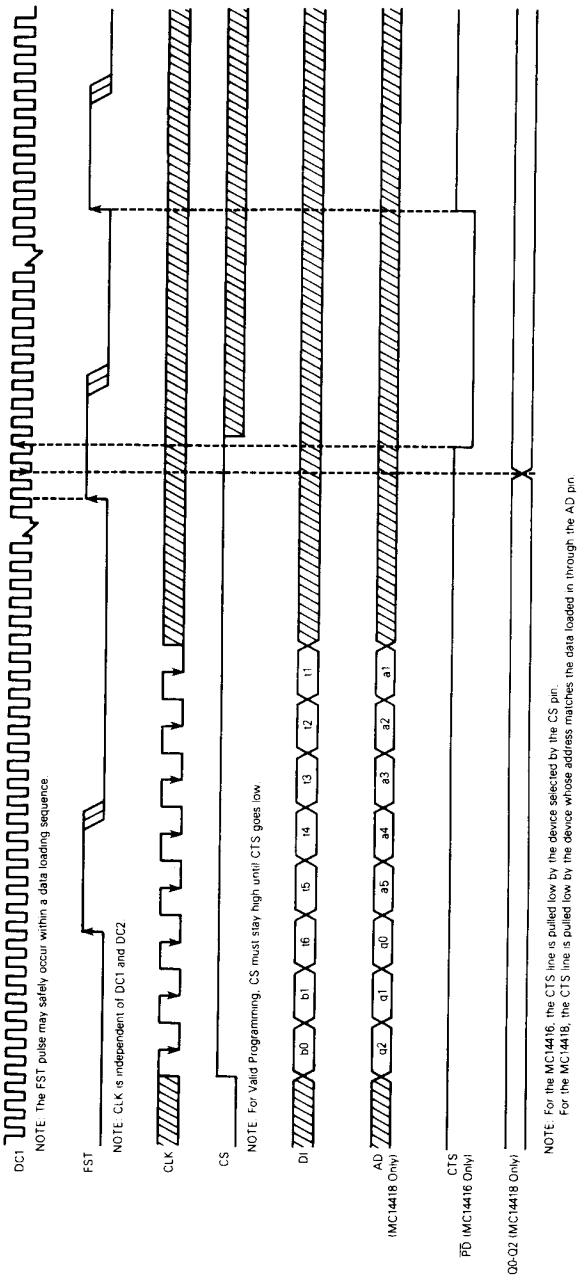
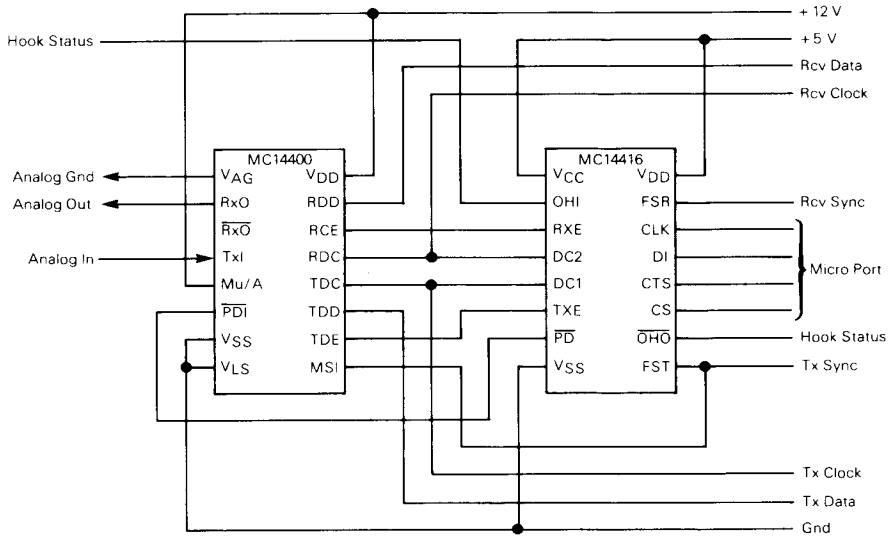


FIGURE 12 — TYPICAL CIRCUIT CONFIGURATION USING MC14416 IN CONJUNCTION WITH MC14400



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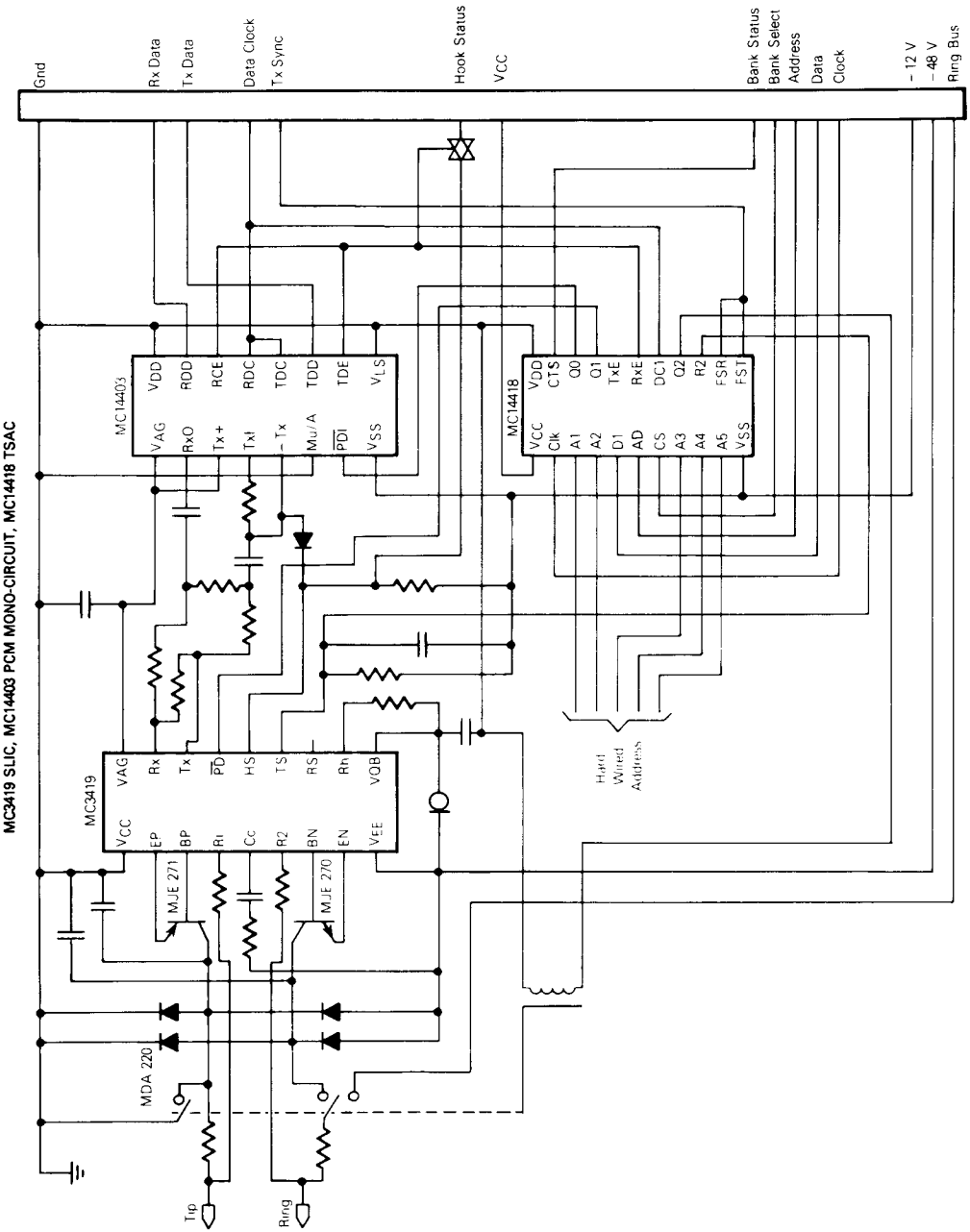
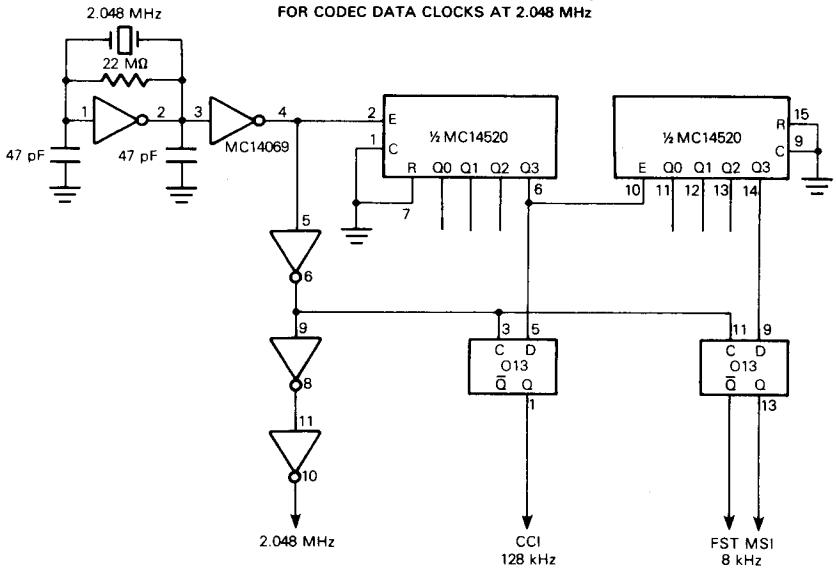


FIGURE 13 — A COMPLETE SINGLE PARTY CHANNEL UNIT USING MC3419 SLIC, MC14403 PCM MONO-CIRCUIT, MC14418 TSAC

FIGURE 14 — CLOCK CIRCUIT AND TIMING
FOR CODEC DATA CLOCKS AT 2.048 MHz



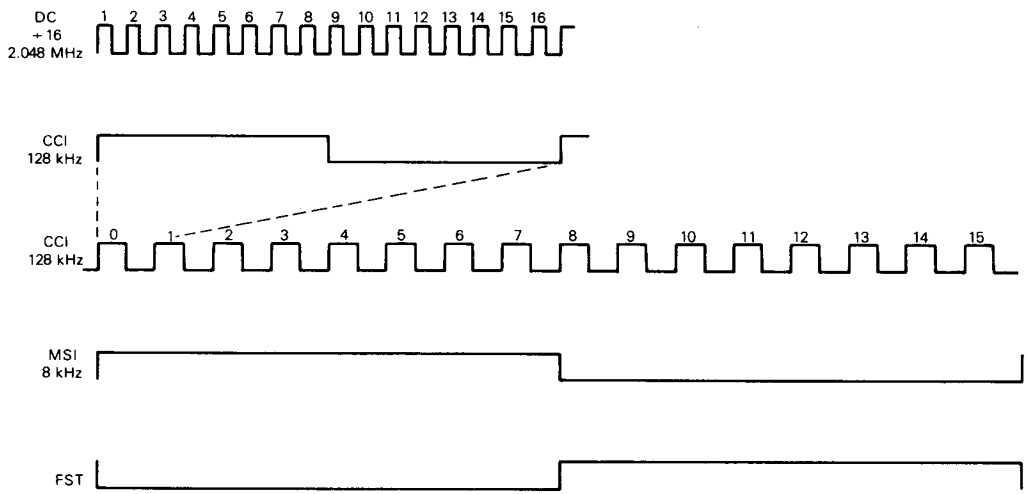


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FIGURE 15 — CLOCK CIRCUIT AND TIMING
FOR CODEC DATA CLOCKS AT 1.544 MHz