

M5M5278DP,J,FP,VP-20V,-25V

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

PRELIMINARY
 Notice: This is not a final specification.
 Some parameter limits are subject to change.

DESCRIPTION

The M5M5278D is a family of 32768-word by 8-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 3.3V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time M5M5278DP,J,FP,VP-20V 20ns(max)
 M5M5278DP,J,FP,VP-25V 25ns(max)
- Low power dissipation Active 132mW(typ)
 Stand-by 330 μW(typ)
- Power down by \bar{S}
- Single 3.3V power supply
- Fully static operation
- Requires neither external clock nor refreshing
- All inputs and outputs are directly TTL compatible
- Easy memory expansion by chip-select (\bar{S}) input
- Output enable(\bar{OE}) prevents data contention in the I/O bus
- All address inputs are changeable with each other

APPLICATION

High-speed memory system

FUNCTION

A write operation is executed during the \bar{S} low, and \bar{W} low overlap time. In this period, address signals must be stable. When \bar{W} is low, the DQ terminals is maintained in the high impedance state.

In a read operation, after setting \bar{W} to high, \bar{S} to low, and \bar{OE} to low, if the address signals are stable, the data is available at the DQ terminals.

When \bar{S} is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Setting \bar{OE} at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

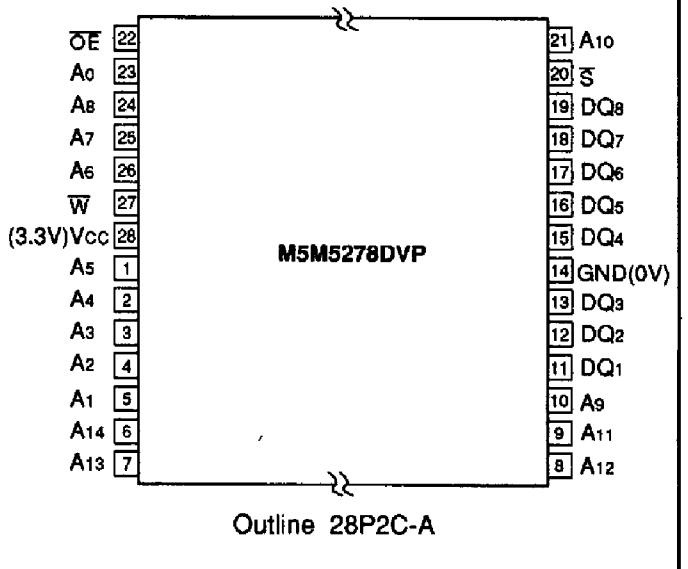
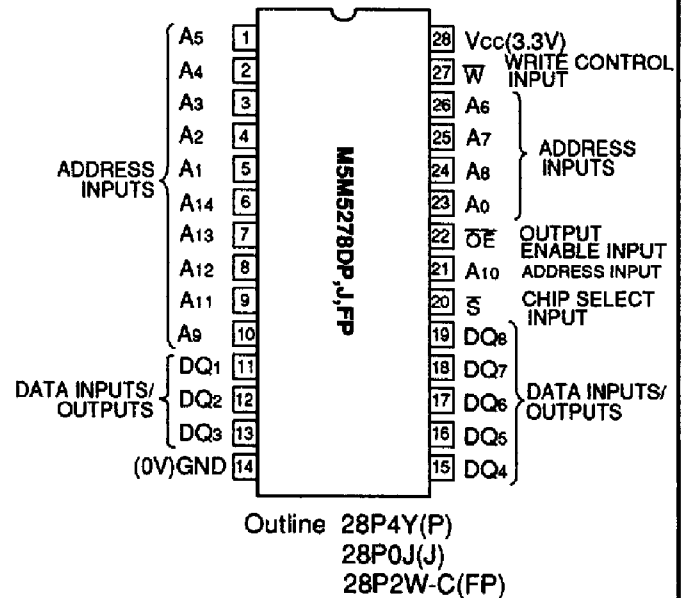
Signal \bar{S} controls the power-down feature. When \bar{S} goes high, power dissipation is reduced extremely. The access time from \bar{S} is equivalent to the address access time.

MODE SELECTION

\bar{S}	\bar{W}	\bar{OE}	Mode	Data input /output	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	Din	Active
L	H	L	Read	Dout	Active
L	H	H		High-impedance	Active

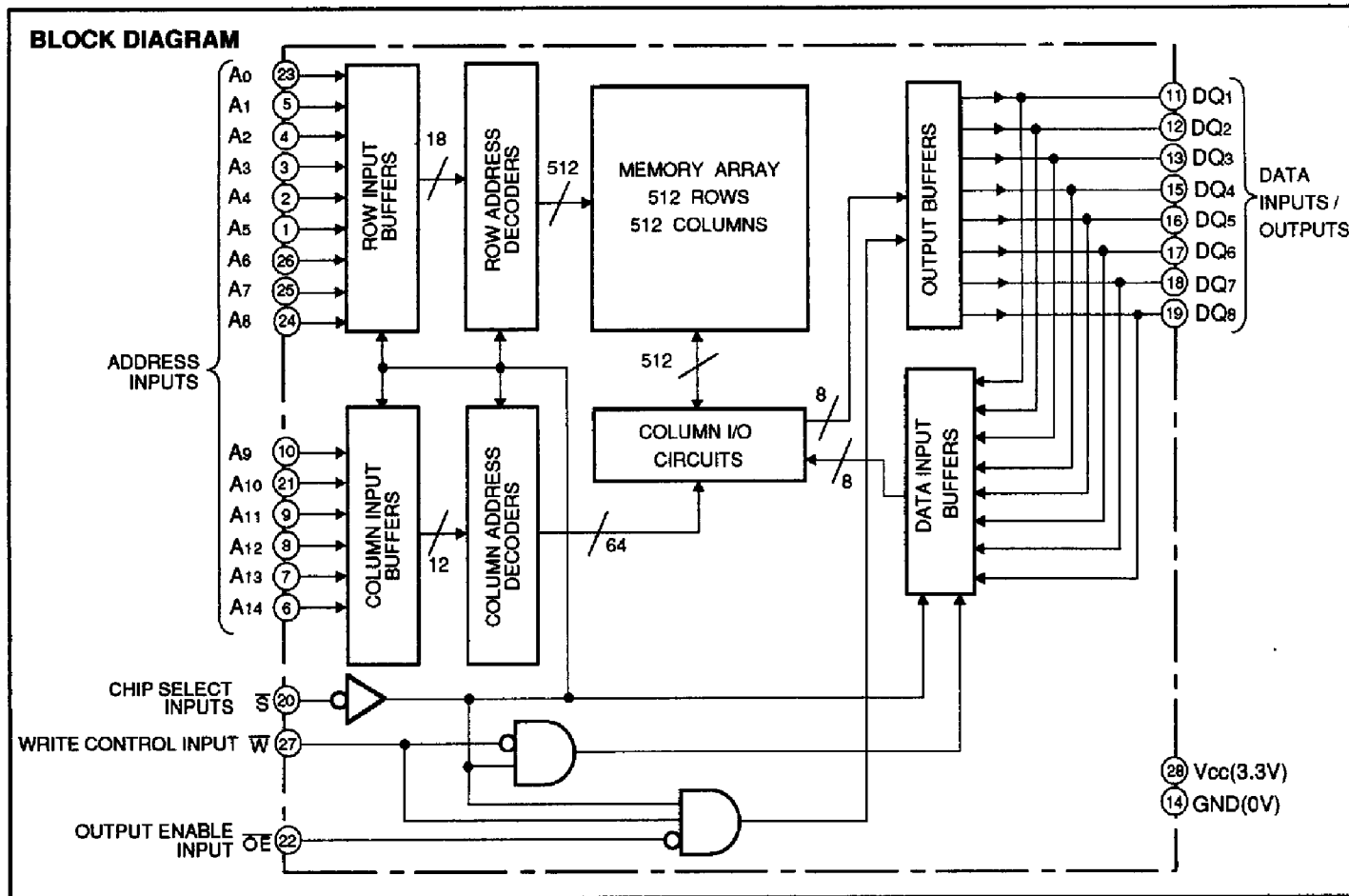
H:VIH L:VIL X:VIH or VIL

PIN CONFIGURATION (TOP VIEW)



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to GND	-3.5~7	V
V _I	Input voltage		-3.5~7	V
V _O	Output voltage		-3.5~7	V
P _d	Maximum power dissipation		1	W
T _{opr}	Operating temperature		0 ~ 70	°C
T _{stg(bias)}	Storage temperature (bias)		-10 ~ 85	°C
T _{stg}	Storage temperature		-65 ~ 150	°C

* Pulse width ≤ 10ns. In case of DC: - 0.5V

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, V_{CC}=3.3V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{IH}	High - level input voltage		2.0		V _{CC} +0.3	V
V _{IL}	Low - level input voltage		-0.3*		0.8	V
V _{OH}	High - level output voltage	I _{OH} = - 4mA	2.4			V
V _{OL}	Low - level output voltage	I _{OL} = 8mA			0.4	V
I _I	Input current	V _I = 0~V _{CC}			2	μA
I _{oz}	Off-state output current	V _{I(s)} = V _{IH} , V _O = 0~V _{CC}			10	μA
I _{CC1}	Supply current from V _{CC}	V _{I(s)} = V _{IL} Output open	AC(20ns cycle)		70	mA
			AC(25ns cycle)		65	
			DC	40	45	
I _{CC2}	Stand-by current	V _{I(s)} = V _{IH}	AC(25ns cycle)		20	mA
			Other V _I ≥ V _{IH} or ≤ V _{IL}		10	
I _{CC3}	Stand-by current	V _{I(s)} = V _{CC} - 0.2V Other V _I ≤ 0.2V or V _I ≥ V _{CC} -0.2V			100	μA

Note 1. Current flow into an IC is positive, out is negative.

* - 3.0V in case of AC (Pulse width ≤ 10ns)

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _I	Input capacitance	V _I = GND, V _I = 25mVrms, f=1MHz			5+	pF
C _O	Output capacitance	V _O = GND, V _O = 25mVrms, f=1MHz			7+	pF

* C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, V_{CC}=3.3V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels V_{IH} = 3.0V, V_{IL} = 0V
 Input rise and fall time 3ns
 Input timing reference levels V_{IH} = 1.5V, V_{IL} = 1.5V
 Output timing reference levels V_{OH} = 1.5V, V_{OL} = 1.5V
 Output loads Fig1, Fig2

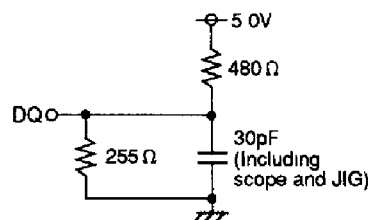


Fig.1 Output load

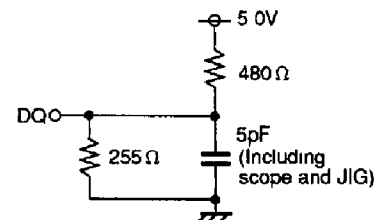


Fig.2 Output load for ten, tdis

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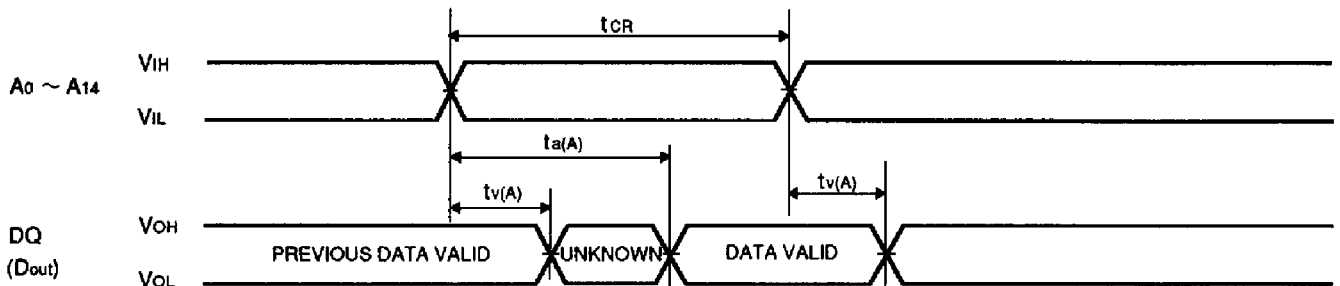
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(2) READ CYCLE

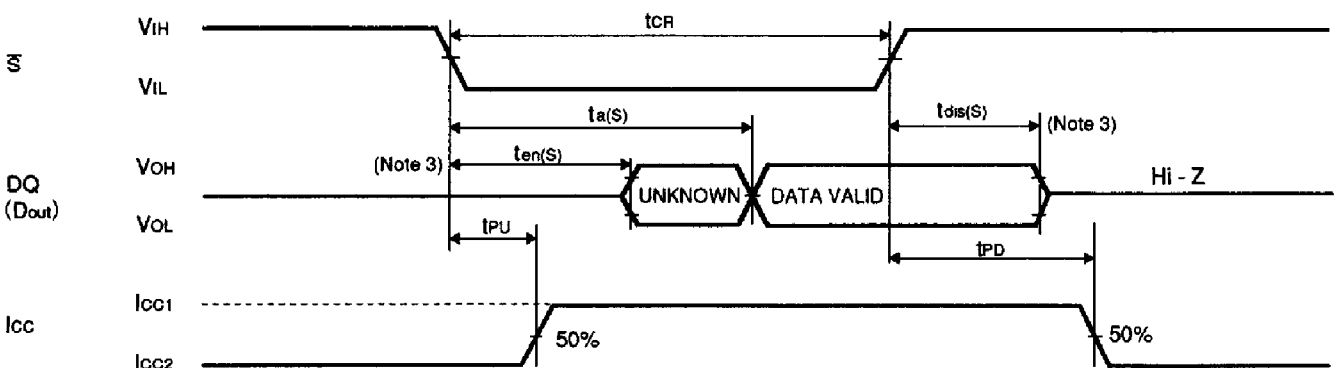
Symbol	Parameter	Limits				Unit
		M5M5278D-20V		M5M5278D-25V		
		Min	Max	Min	Max	
t _{CR}	Read cycle time	20		25		ns
t _{a(A)}	Address access time		20		25	ns
t _{a(S)}	Chip select access time		20		25	ns
t _{a(OE)}	Output enable access time		10		12	ns
t _{v(A)}	Data valid time after address change	3		5		ns
t _{en(S)}	Output enable time after \overline{S} low	3		5		ns
t _{dis(S)}	Output disable time after \overline{S} high	0	8	0	10	ns
t _{en(OE)}	Output enable time after \overline{OE} low	0		0		ns
t _{dis(OE)}	Output disable time after \overline{OE} high	0	8	0	10	ns
t _{PU}	Power-up time after chip selection	0		0		ns
t _{PD}	Power-down time after chip deselection		20		25	ns

(3) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1 < $\overline{W}=H, \overline{S}=L$ >

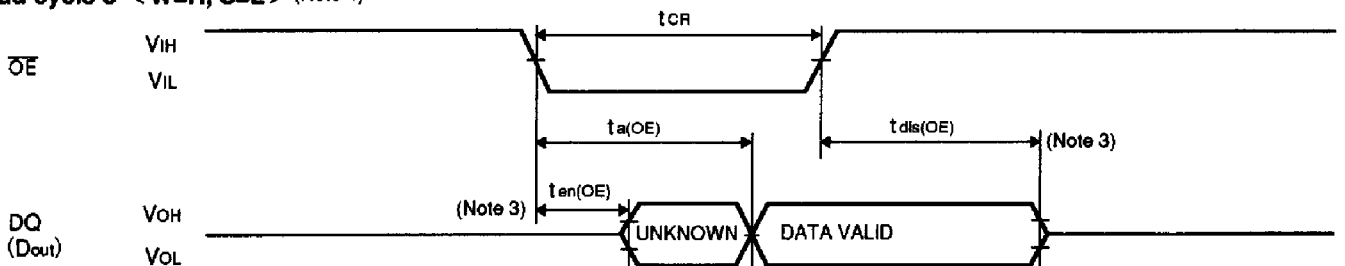


Read cycle 2 < $\overline{W}=H$ > (Note 2)



Note 2. Address valid prior to or coincident with \overline{S} transition low.
3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Figure 2.

Read cycle 3 < $\overline{W}=H, \overline{S}=L$ > (Note 4)



Note 4. Address and \overline{S} valid prior to \overline{OE} transition low by $(t_{a(A)} - t_{a(OE)})$, $(t_{a(S)} - t_{a(OE)})$.

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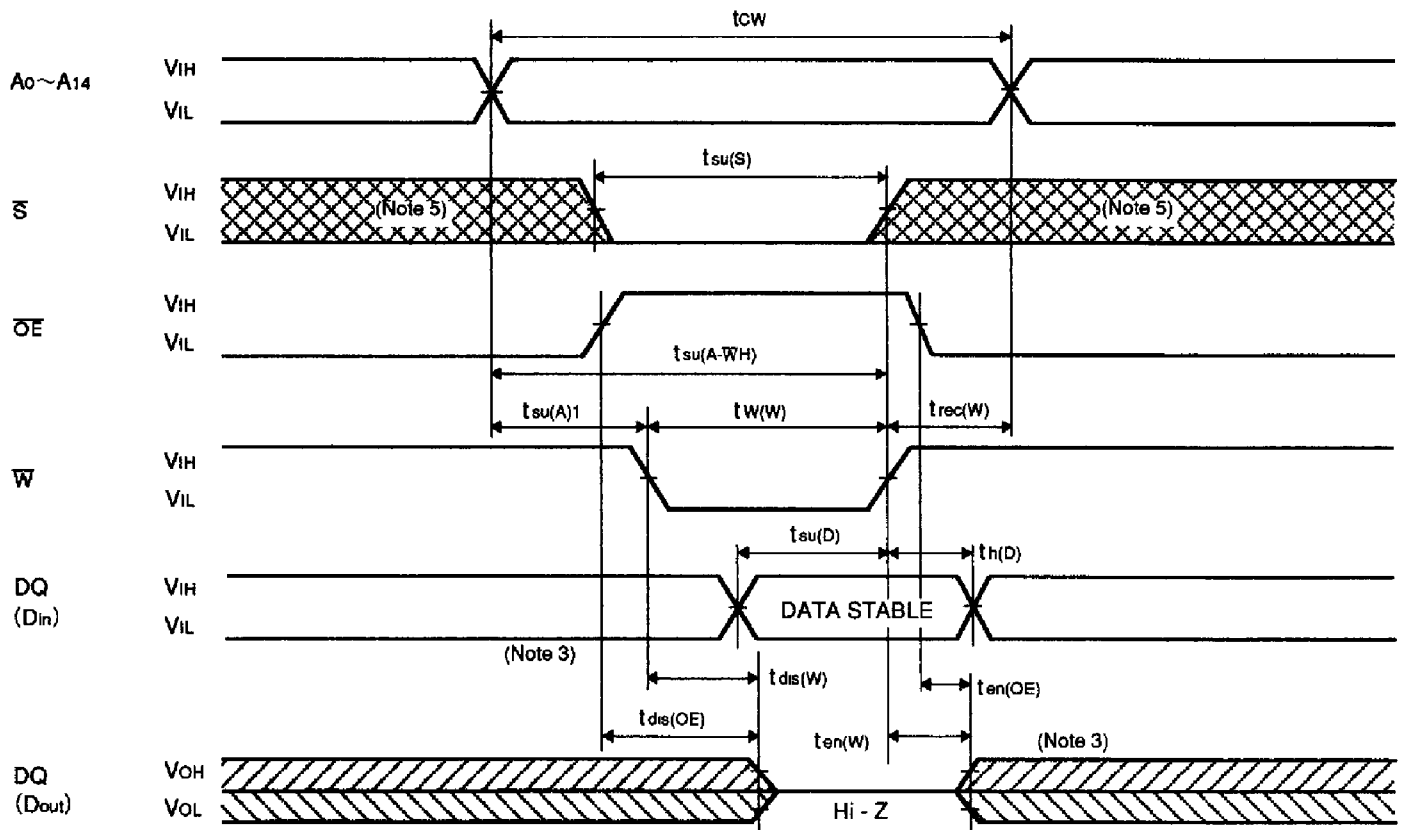
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(4) WRITE CYCLE

Symbol	Parameter	Limits				Unit
		M5M5278D-20V		M5M5278D-25V		
		Min	Max	Min	Max	
t_{cw}	Write cycle time	20		25		ns
$t_{su}(S)$	Chip select setup time	15		20		ns
$t_{su}(A)1$	Address setup time 1 (\overline{W} CONTROL)	0		0		ns
$t_{su}(A)2$	Address setup time 2 (\overline{S} CONTROL)	0		0		ns
$t_w(W)$	Write pulse width	15		20		ns
$t_{rec}(W)$	Write recovery time	0		0		ns
$t_{su}(D)$	Data setup time	8		10		ns
$t_h(D)$	Data hold time	0		0		ns
$t_{dis}(W)$	Output disable time after \overline{W} low	0	8	0	10	ns
$t_{en}(W)$	Output enable time after \overline{W} high	0		0		ns
$t_{su}(A-WH)$	Address to \overline{W} high	15		20		ns
$t_{en}(OE)$	Output enable time after \overline{OE} low	0		0		ns
$t_{dis}(OE)$	Output disable time after \overline{OE} high	0	8	0	10	ns

(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 (\overline{W} control mode)

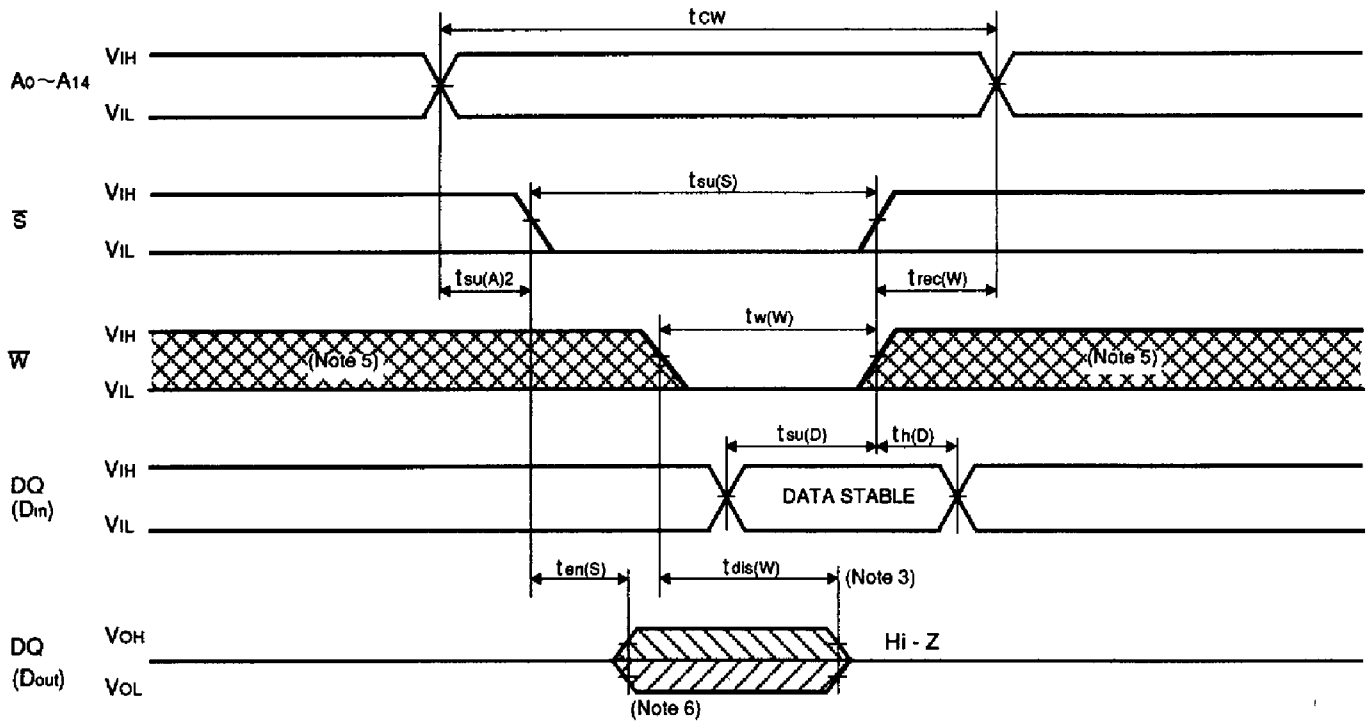


Note 5. Hatching indicates the state is don't care.

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Write cycle 2 (\bar{S} control mode)



Note 6. When the falling edge of \bar{W} is simultaneous or prior to the falling edge of \bar{S} , the output is maintained in the high impedance.
 7. t_{en} , t_{dis} are periodically sampled and are not 100% tested.