

# M5M5256DP, KP, FP, VP, RV -45LL-I, -55LL-I, -70LL-I, -45XL-I, -55XL-I, -70XL-I

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

## DESCRIPTION

The M5M5256DP, KP, FP, VP, RV is 262,144-bit CMOS static RAMs organized as 32,768-words by 8-bits which is fabricated using high-performance 3 polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery results in a high density and low power static RAM. Stand-by current is small enough for battery back-up application. It is ideal for the memory systems which require simple interface.

Especially the M5M5256DVP, RV are packaged in a 28-pin thin small outline package. Two types of devices are available, M5M5256DVP (normal lead bend type package), M5M5256DRV (reverse lead bend type package). Using both types of devices, it becomes very easy to design a printed circuit board.

## FEATURE

Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5256DP, KP, FP, VP, RV-45LL	45ns	55mA (V <sub>CC</sub> =5.5V)	40µA (V <sub>CC</sub> =5.5V)
M5M5256DP, KP, FP, VP, RV-55LL	55ns		
M5M5256DP, KP, FP, VP, RV-70LL	70ns		
M5M5256DP, KP, FP, VP, RV-45XL	45ns	10µA (V <sub>CC</sub> =5.5V)	0.05µA (V <sub>CC</sub> =3.0V, Typical)
M5M5256DP, KP, FP, VP, RV-55XL	55ns		
M5M5256DP, KP, FP, VP, RV-70XL	70ns		

- Single +5V power supply
- No clocks, no refresh
- Data-Hold on +2.0V power supply
- Directly TTL compatible : all inputs and outputs
- Three-state outputs : OR-tie capability
- /OE prevents data contention in the I/O bus
- Common Data I/O
- Battery backup capability
- Low stand-by current.....0.05µA(typ.)

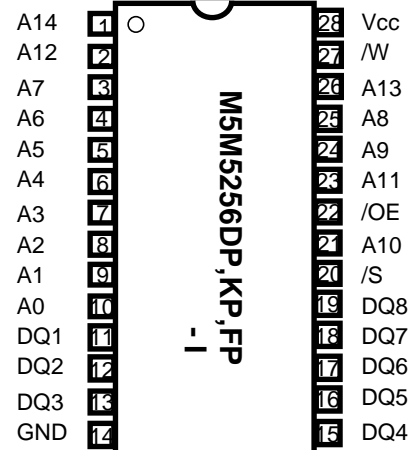
## PACKAGE

M5M256DP : 28 pin 600 mil DIP  
 M5M5256DKP : 28 pin 300 mil DIP  
 M5M5256DFP : 28 pin 450 mil SOP  
 M5M5256DVP, RV : 28pin 8 X 13.4 mm<sup>2</sup> TSOP

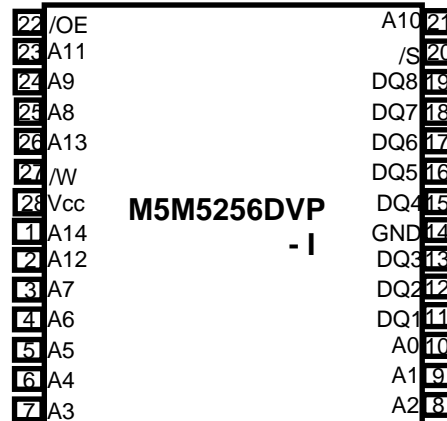
## APPLICATION

Small capacity memory units

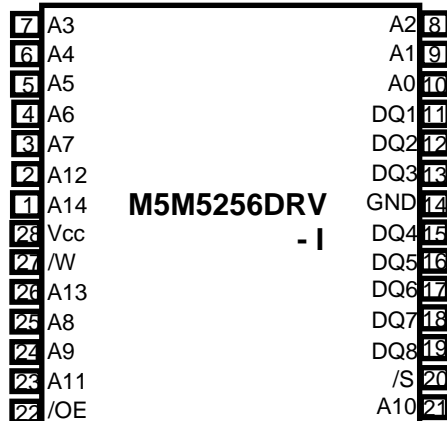
### PIN CONFIGURATION (TOP VIEW)



Outline 28P4 (DP)  
 28P4Y (DKP)  
 28P2W-C (DFP)



Outline 28P2C-A (DVP)



Outline 28P2C-B (DRV)

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## FUNCTION

The operation mode of the M5M5256DP, KP, FP, VP, RV is determined by a combination of the device control inputs /S, /W and /OE. Each mode is summarized in the function table.

A write cycle is executed whenever the low level /W overlaps with the low level /S. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of /W, /S, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable /OE directly controls the output stage. Setting the /OE at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

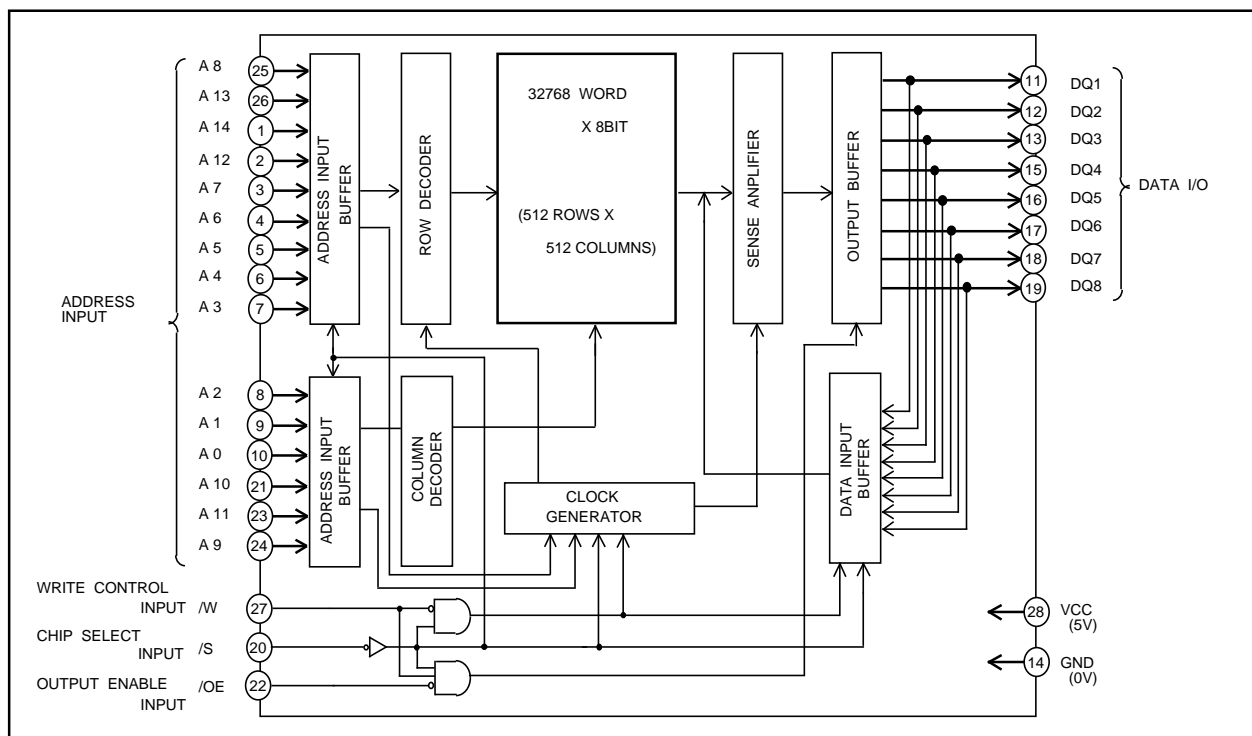
A read cycle is executed by setting /W at a high level and /OE at a low level while /S are in an active state.

When setting /S at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by /S. The power supply current is reduced as low as the stand-by current which is specified as Icc3 or Icc4, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

## FUNCTION TABLE

/S	/W	/OE	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	DIN	Active
L	H	L	Read	DOUT	Active
L	H	H		High-impedance	Active

## BLOCK DIAGRAM



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-45XL-I, -55XL-I, -70XL-I**

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**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>cc</sub>	Supply voltage	With respect to GND	-0.3*~7.0	V
V <sub>i</sub>	Input voltage		-0.3*~V <sub>cc</sub> +0.3 (Max 7.0)	V
V <sub>o</sub>	Output voltage		0~V <sub>cc</sub>	V
P <sub>d</sub>	Power dissipation	T <sub>a</sub> =25°C	700	mW
T <sub>opr</sub>	Operating temperature		-40~85	°C
T <sub>stg</sub>	Storage temperature		-65~150	°C

\* -3.0V in case of AC ( Pulse width 30ns )

**DC ELECTRICAL CHARACTERISTICS** (T<sub>a</sub>=-40~85°C, V<sub>cc</sub>=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V <sub>IH</sub>	High-level input voltage		2.2		V <sub>cc</sub> +0.3	V
V <sub>IL</sub>	Low-level input voltage		-0.3		0.8	V
V <sub>OH1</sub>	High-level output voltage 1	I <sub>OH</sub> =-1mA	2.4			V
V <sub>OH2</sub>	High-level output voltage 2	I <sub>OH</sub> =-0.1mA	V <sub>cc</sub> -0.5			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> =2mA			0.4	V
I <sub>i</sub>	Input current	V <sub>i</sub> =0~V <sub>cc</sub>			±1	uA
I <sub>o</sub>	Output current in off-state	/S=V <sub>IH</sub> or or /OE=V <sub>IH</sub> , V <sub>I/O</sub> =0~V <sub>cc</sub>			±1	uA
I <sub>cc1</sub>	Active supply current (AC, MOS level )	/S 0.2V, Other inputs<0.2V or >V <sub>cc</sub> -0.2V Output-open Min. cycle	45ns	35	50	mA
			55ns	30	45	
			70ns	25	40	
I <sub>cc2</sub>	Active supply current (AC, TTL level )	/S=V <sub>IL</sub> , other inputs=V <sub>IH</sub> or V <sub>IL</sub> Output-open Min. cycle	45ns	35	55	mA
			55ns	30	50	
			70ns	25	45	
I <sub>cc3</sub>	Stand-by current	/S V <sub>cc</sub> -0.2V, other inputs=0~V <sub>cc</sub>	-LL		40	uA
			-XL	0.1	10	
I <sub>cc4</sub>	Stand-by current	/S=V <sub>IH</sub> , other inputs=0~V <sub>cc</sub>			3	mA

\* -3.0V in case of AC ( Pulse width 30ns )

**CAPACITANCE** (T<sub>a</sub>=-40~85°C, V<sub>cc</sub>=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C <sub>i</sub>	Input capacitance	V <sub>i</sub> =GND, V <sub>i</sub> =25mVrms, f=1MHz			6	pF
C <sub>o</sub>	Output capacitance	V <sub>o</sub> =GND, V <sub>o</sub> =25mVrms, f=1MHz			8	pF

Note 0: Direction for current flowing into an IC is positive (no mark).

1: Typical value is one at T<sub>a</sub> = 25°C.

2: C<sub>i</sub>, C<sub>o</sub> are periodically sampled and are not 100% tested.

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## AC ELECTRICAL CHARACTERISTICS (Ta = -40~85°C, Vcc=5V±10%, unless otherwise noted)

### (1) MEASUREMENT CONDITIONS

Input pulse level.....V<sub>IH</sub>=2.4V, V<sub>IL</sub>=0.6V

Input rise and fall time.....5ns

Reference level.....V<sub>OH</sub>=V<sub>OL</sub>=1.5V

Output loads.....Fig.1, CL=30pF (-45LL, -45XL)  
 CL=50pF (-55LL, -55XL)  
 CL=100pF (-70LL, -70XL)  
 CL=5pF (for ten, tdis)

Transition is measured ±500mV from steady state voltage. (for ten, tdis)

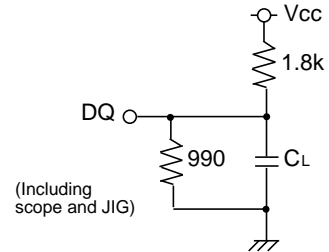


Fig.1 Output load

### (2) READ CYCLE

Symbol	Parameter	Limits						Unit
		-45LL, XL		-55LL, XL		-70LL, XL		
		Min	Max	Min	Max	Min	Max	
t <sub>CR</sub>	Read cycle time	45		55		70		ns
t <sub>a(A)</sub>	Address access time		45		55		70	ns
t <sub>a(S)</sub>	Chip select access time		45		55		70	ns
t <sub>a(OE)</sub>	Output enable access time		25		30		35	ns
t <sub>dis(S)</sub>	Output disable time after /S high		15		20		25	ns
t <sub>dis(OE)</sub>	Output disable time after /OE high		15		20		25	ns
t <sub>en(S)</sub>	Output enable time after /S low	5		5		5		ns
t <sub>en(OE)</sub>	Output enable time after /OE low	5		5		5		ns
t <sub>v(A)</sub>	Data valid time after address	10		10		10		ns

### (3) WRITE CYCLE

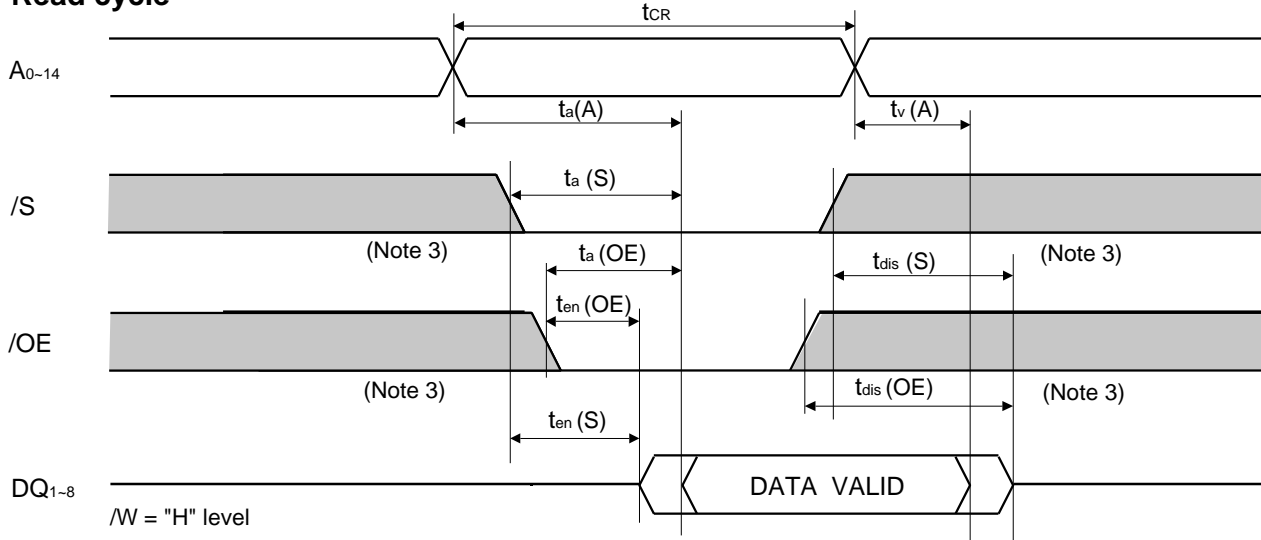
Symbol	Parameter	Limits						Unit
		-45LL, XL		-55LL, XL		-70LL, XL		
		Min	Max	Min	Max	Min	Max	
t <sub>cw</sub>	Write cycle time	45		55		70		ns
t <sub>w(W)</sub>	Write pulse width	35		40		50		ns
t <sub>su(A)</sub>	Address setup time	0		0		0		ns
t <sub>su(A-WH)</sub>	Address setup time with respect to /W high	40		50		65		ns
t <sub>su(S)</sub>	Chip select setup time	40		50		65		ns
t <sub>su(D)</sub>	Data setup time	20		25		30		ns
t <sub>h(D)</sub>	Data hold time	0		0		0		ns
t <sub>rec(W)</sub>	Write recovery time	0		0		0		ns
t <sub>dis(W)</sub>	Output disable time from /W low		15		20		25	ns
t <sub>dis(OE)</sub>	Output disable time from /OE high		15		20		25	ns
t <sub>en(W)</sub>	Output enable time from /W high	5		5		5		ns
t <sub>en(OE)</sub>	Output enable time from /OE low	5		5		5		ns

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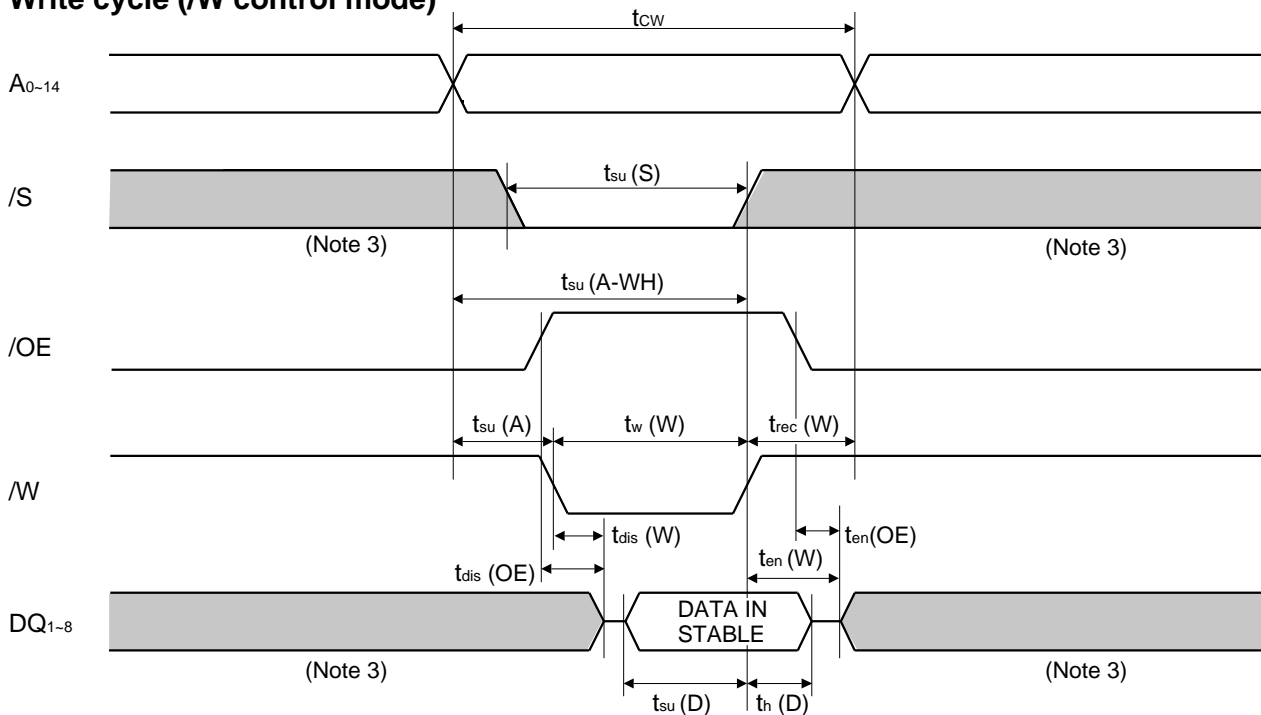
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**(4) TIMING DIAGRAMS**

**Read cycle**



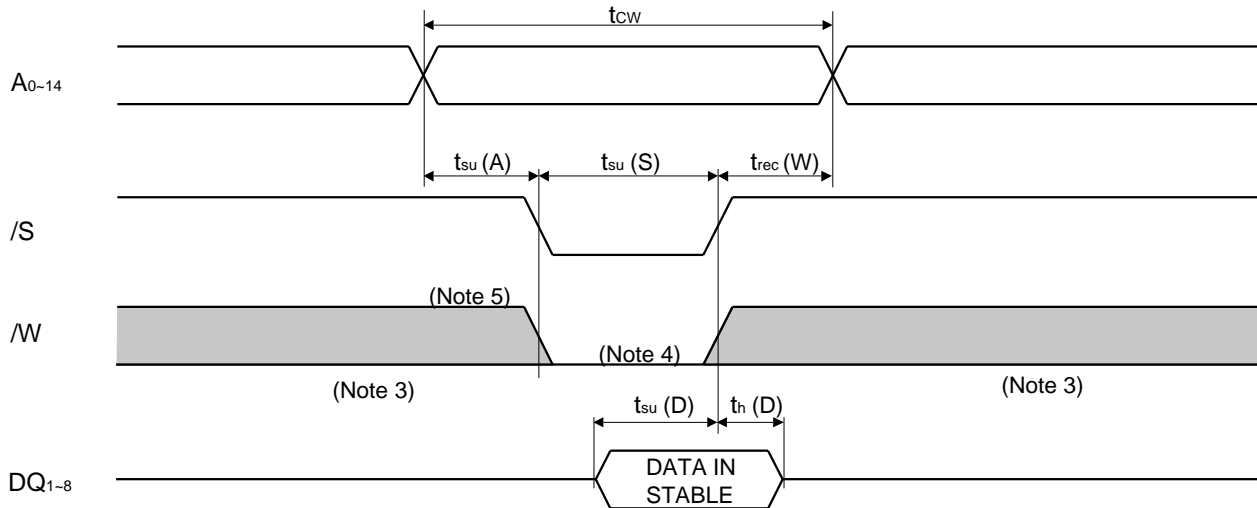
**Write cycle (/W control mode)**



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**Write cycle (/S control mode)**



- Note 3 : Hatching indicates the state is "don't care".
- 4 : Writing is executed in overlap of /S and /W low.
- 5 : If /W goes low simultaneously with or prior to /S, the outputs remain in the high impedance state.
- 6 : Don't apply inverted phase signal externally when DQ pin is output mode.
- 7 :  $t_{en}$ ,  $t_{dis}$  are periodically sampled and are not 100% tested.

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## POWER DOWN CHARACTERISTICS

### (1) ELECTRICAL CHARACTERISTICS (Ta = -40~85°C, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V <sub>CC (PD)</sub>	Power down supply voltage		2			V
V <sub>I (/S)</sub>	Chip select input /S	2.2V V <sub>CC(PD)</sub>	2.2			V
		2V V <sub>CC(PD)</sub> 2.2V		V <sub>CC(PD)</sub>		V
I <sub>CC (PD)</sub>	Power down supply current	V <sub>CC</sub> = 3V, /S V <sub>CC</sub> -0.2V, Other inputs=0~V <sub>CC</sub>	-LL		20 (Note 7)	uA
			-XL	0.05	4 (Note 8)	

Note7: I<sub>CC (PD)</sub> = 1uA in case of Ta = 25°C

Note8: I<sub>CC (PD)</sub> = 0.2uA in case of Ta = 25°C

### (2) TIMING REQUIREMENTS (Ta = -40~85°C, Vcc=5V±10%, unless otherwise noted )

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t <sub>su (PD)</sub>	Power down set up time		0			ns
t <sub>rec (PD)</sub>	Power down recovery time		t <sub>CR</sub>			ns

### (3) POWER DOWN CHARACTERISTICS

#### /S control mode

