ANALOG DEVICES

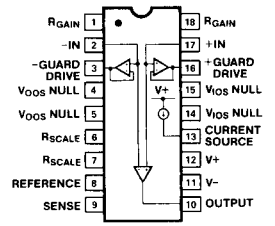
Fast Settling JFET Instrumentation Amplifier

AMP-05

FEATURES

- Settling-Time to 12-Bit Accuracy, G ≤ 2000 ..... 15μs Max
- Overload Recovery Time, G = 1000 ..... 15μs
- 14-Bit Gain Linearity at G ≤ 1000
- On-Board Dual Guard Drivers
- On-Board 100μA Precision Current Source
- Low Bias Current ..... 50pA Max @ 25°C
  ..... 20nA Max @ 125°C
- Temperature Stable CMR
  ..... 105dB Min Over −55°C to +125°C
- High Slew-Rate with 500pF Load ..... 5V/μs Min
- Input Overload Protected to ±30V Differential
- Available in Die Form

PIN CONNECTIONS



18-PIN HERMETIC DIP
(X-Suffix)

4

ORDERING INFORMATION†

CERDIP 18-PIN PACKAGE	OPERATING TEMPERATURE RANGE
AMP05AX*	MIL
AMP05BX*	MIL
AMP05EX	IND
AMP05FX	IND

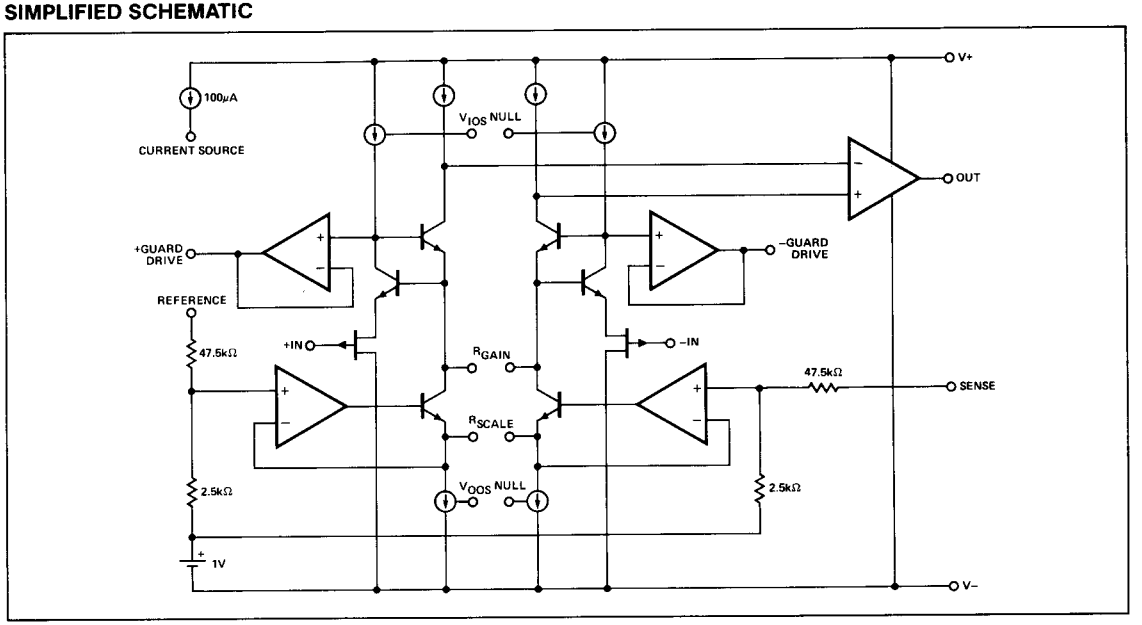
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The AMP-05 is a fast JFET instrumentation amplifier designed for high-speed analog signal-processing and analog-multiplexed data acquisition systems. Settling-time to 12-bits is 15μs maximum, with better than 14-bit linearity at all gains up to 1000. Two functions are added to the instrumentation amplifier that reduce external component count in many applications. On-board dual guard drivers maintain good settling-time and common-mode rejection performance when shielded cable connects the input signal to the AMP-05. A precision 100μA current source is also provided for transducer excitation, powering a low-current voltage reference, and other functions.

SIMPLIFIED SCHEMATIC



AMP-05

The AMP-05 employs a current-feedback technique which provides a high and stable common-mode rejection, 105dB minimum over the military temperature range. JFET inputs reduce bias current to 50pA maximum at 25°C and only 20nA maximum at 125°C; low bias current reduces errors due to signal-source resistance. Internal input protection allows a 30V differential overload at all gain settings. The AMP-05 recovers rapidly when an input overload is removed. Recovery time is typically 15μs following a 1000:1 overload, voltage gain set to 1000. AMP-05 voltage gain is set by the ratio of two external resistors over the range 0.1 to 2000 and a low gain temperature-coefficient of 20ppm/°C maximum is achievable in the range 1 to 1000.

The AMP-05's outputs can all drive large capacitive loads without oscillation. The amplifier output is guaranteed stable with loads up to 2,000pF and the guard drivers can tolerate up to 10,000pF without oscillation.

Sense and reference pins complete the output feedback-loop and provide an output ground reference, respectively. The reference pin may be used for zeroing system offsets, where auto-zero hardware is employed. Resistance in series with the reference terminal does not degrade common-mode rejection on PMI's AMP-05, which is a significant problem with instrumentation amplifiers employing the three op-amp configuration.

For applications requiring very low input offset voltage and low offset drift, or higher output drive capability, refer to the AMP-01 data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Common-Mode Input Voltage ..... Supply Voltage
Differential Input Voltage ..... ±30V
(Inputs must not exceed supply voltages.)
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range
AMP-05A, B ..... –55°C to +125°C
AMP-05E, F ..... –25°C to +85°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_J) ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
18-Pin Hermetic DIP (X)	74	7	°C/W

NOTES:
1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 5k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

			AMP-05A/E			AMP-05B/F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
GAIN									
Gain Range	G_R		0.1	—	2000	0.1	—	2000	
Gain Equation Accuracy		$G = 20 \times R_S/R_G$ G = 1 to 1000	—	0.25	0.5	—	0.4	1.0	%
Gain Nonlinearity	G_{NL}	G = 1	—	0.001	—	—	0.001	—	%
		G = 10	—	0.002	—	—	0.002	—	
		G = 100	—	0.007	—	—	0.007	—	
		G = 1000	—	0.020	—	—	0.020	—	
		$R_L = 10k\Omega$ G = 100	—	0.004	—	—	0.004	—	%
		G = 1000	—	0.004	—	—	0.004	—	
Gain Temperature Coefficient	G_{TC}	G = 1 to 100	—	1.7	10	—	1.7	10	ppm/°C
		G = 1000 (Notes 1, 2)	—	8	20	—	8	20	
OUTPUT RATING									
Output Voltage Swing	V_{OUT}	$R_L = 1k\Omega$	±11	±12	—	±11	±12	—	V
		Over Temperature	±10.5	±12	—	±10.5	±12	—	
Short Circuit Current	I_{SC}	Output Shorted to Ground	±20	±35	—	±20	±35	—	mA
Capacitive Load Stability		Full Gain Range No Oscillations	2	10	—	2	10	—	nF

NOTES:
1. Gain tempco does not include the effects of gain and scale resistor tempco match.
2. Guaranteed but not 100% production tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 5k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	AMP-05A/E MIN	AMP-05A/E TYP	AMP-05A/E MAX	AMP-05B/F MIN	AMP-05B/F TYP	AMP-05B/F MAX	UNITS
INPUT									
Input Bias Current	I_B	$T_A \leq 25°C$	—	20	50	—	30	100	pA
		$T_A = 85°C$ (E/F Grades)	—	0.5	4	—	1	8	nA
		$T_A = 125°C$ (A/B Grades)	—	7	20	—	12	30	nA
Input Offset Current	I_{OS}	$T_A \leq 25°C$	—	5	25	—	10	50	pA
		$T_A = 85°C$ (E/F Grades)	—	0.05	0.5	—	0.1	1	nA
		$T_A = 125°C$ (A/B Grades)	—	1	5	—	2	10	nA
Input Resistance	R_{IN}		—	10^{12}	—	—	10^{12}	—	Ω
Input Capacitance	C_{IN}		—	8	—	—	8	—	pF
Input Voltage Range	IVR	$T_A = 25°C$	±11	±11.5	—	±11	±11.5	—	V
		Over Temperature	±10	±11	—	±10	±11	—	
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$							
		G = 1000	110	115	—	100	110	—	dB
		G = 100	105	115	—	95	110	—	
		G = 10	100	110	—	90	100	—	
		G = 1	90	98	—	80	90	—	
		$V_{CM} = \pm 10V$, Over Temperature							
		G = 1000	105	110	—	95	105	—	dB
		G = 100	100	110	—	90	105	—	
		G = 10	95	105	—	85	95	—	
		G = 1	85	95	—	75	85	—	
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}	$V_{CM} = 0V$							
		$T_A = 25°C$	—	0.3	1.0	—	0.5	2.0	mV
		Over Temperature	—	0.8	2.0	—	1.0	4.0	
Input Offset Voltage Drift	TCV_{IOS}		—	5	10	—	7	20	μV/°C
Output Offset Voltage	V_{OOS}	$T_A = 25°C$	—	3	15	—	5	25	mV
		Over Temperature	—	9	25	—	11	40	
Output Offset Voltage Drift	TCV_{OOS}		—	50	100	—	70	150	μV/°C
Offset Referred to Input vs. Positive Supply V+ = +5V to +15V	+PSR	G = 1000	115	120	—	110	115	—	dB
		G = 100	110	118	—	105	110	—	
		G = 10	95	105	—	90	100	—	
		G = 1	75	85	—	70	80	—	
		Over Temperature							
		G = 1000	110	116	—	105	110	—	dB
		G = 100	105	114	—	100	105	—	
		G = 10	90	102	—	85	98	—	
		G = 1	75	84	—	70	80	—	
Offset Referred to Input vs. Negative Supply V− = −5V to −15V	−PSR	G = 1000	110	118	—	105	110	—	dB
		G = 100	95	104	—	90	98	—	
		G = 10	75	84	—	70	80	—	
		G = 1	55	64	—	50	60	—	
		Over Temperature							
		G = 1000	105	113	—	100	105	—	dB
		G = 100	95	104	—	90	95	—	
		G = 10	75	84	—	70	80	—	
		G = 1	55	64	—	50	60	—	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 5k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	AMP-05A/E MIN	AMP-05A/E TYP	AMP-05A/E MAX	AMP-05B/F MIN	AMP-05B/F TYP	AMP-05B/F MAX	UNITS
Input Offset Voltage Trim Range		$V_S = \pm 4.5V$ to $\pm 18V$	±2.5	±5	—	±2.5	±5	—	mV
Output Offset Voltage Trim Range		$V_S = \pm 4.5V$ to $\pm 18V$	±25	±40	—	±25	±40	—	mV
SENSE INPUT									
Input Resistance	R_{IN}		40	50	60	40	50	60	kΩ
Input Current	I_{IN}	Referenced to V–	—	280	—	—	280	—	μA
REFERENCE INPUT									
Input Resistance	R_{IN}		40	50	60	40	50	60	kΩ
Input Current	I_{IN}	Referenced to V–	—	280	—	—	280	—	μA
Voltage Range			−10.5	—	+20	−10.5	—	+20	V
Gain to Output			—	1	—	—	1	—	V/V
NOISE									
Voltage Density RTI	e_n	$f_O = 1kHz$ $G \geq 100$ $G = 10$ $G = 1$	— — —	16 38 350	— — —	— — —	16 38 350	— — —	$nV/\sqrt{Hz}$
Noise Current Density	i_n	$f_O = 1kHz$	—	10	—	—	10	—	$fA/\sqrt{Hz}$
Input Noise Voltage	e_{np-p}	Measured at G = 1000, 0.1Hz to 10Hz Bandwidth	—	4	—	—	4	—	μV_{p-p}
Output Noise Voltage	e_{np-p}	Measured at G = 0, 0.1Hz to 10Hz Bandwidth	—	7	—	—	7	—	μV_{p-p}
Input Noise Current	i_{np-p}	0.1Hz to 10Hz Bandwidth	—	0.12	—	—	0.12	—	pA_{p-p}
DYNAMIC RESPONSE									
Small Signal Bandwidth (−3dB)	BW	$G = 1$ $G \geq 10$	— —	3 120	— —	— —	3 120	— —	MHz kHz
Slew Rate	SR	$C_L = 500pF$ $G \geq 10$ Over Temperature	5 3.5	7.5 5.5	— —	5 3.5	7.5 5.5	— —	V/μs
Settling Time	t_S	$1 \leq G \leq 2000$ −10V to +10V Step (Note 1) to 0.1% to 0.05% to 0.025%	— — —	5 7 10	7 10 15	— — —	5 7 10	7 10 15	μs
Overload Recovery Time	t_{rec}	$G = 1000$ $V_{IN} = 10V$ to 10mV	—	15	—	—	15	—	μs

NOTE:
1. Guaranteed but not 100% production tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 5k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	AMP-05A/E MIN	AMP-05A/E TYP	AMP-05A/E MAX	AMP-05B/F MIN	AMP-05B/F TYP	AMP-05B/F MAX	UNITS
GUARD DRIVERS									
Output Voltage	V_O	Volts above respective input over temperature.	0.5	1.2	2.0	0.5	1.2	2.0	V
Peak Output Current			8	15	—	8	15	—	mA
Slew Rate	SR	C_L = 1000pF	—	16	—	—	16	—	V/μs
Capacitive Load Stability		No Oscillations (Note 1)	10	100	—	10	100	—	nF
CURRENT SOURCE									
Current Output	I_{OUT}	Over Full Compliance Range	90	100	120	90	100	120	μA
Output Compliance Range		V_{OC} Volts Below V+ (Irrespective of V−)	4	—	30	4	—	30	V
Output Impedance	R_{OUT}	Over Full Compliance Range (Note 1)	1	3	—	1	3	—	GΩ
Temperature Coefficient			—	100	—	—	100	—	ppm/°C
Power Supply Rejection			—	150	—	—	150	—	nA/V
POWER SUPPLY $-25°C \le T_A \le +85°C$ for E/F Grades, $-55°C \le T_A \le +125°C$ for A/B Grades									
Supply Voltage Range	V_S		±4.5	—	±18	±4.5	—	±18	V
Quiescent Current	I_Q		—	7.0	9.0	—	7.5	10.0	mA

NOTE:
1. Guaranteed but not 100% production tested.

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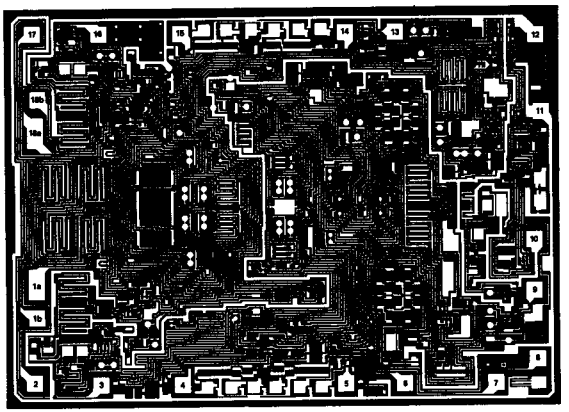
AMP-05

DICE CHARACTERISTICS



DIE SIZE 0.127 × 0.176 inch, 22,352 sq. mils
(3.23 × 4.47mm, 14.42 sq. mm)

1a. R_{GAIN} SENSE
1b. R_{GAIN} FORCE
2. −INPUT
3. −GUARD DRIVE
4. V_{OOS} NULL
5. V_{OOS} NULL
6. R_{SCALE}
7. R_{SCALE}
8. REFERENCE
9. SENSE
10. OUTPUT
11. V−
12. V+
13. CURRENT SOURCE
14. V_{IOS} NULL
15. V_{IOS} NULL
16. +GUARD DRIVE
17. +INPUT
18a. R_{GAIN} SENSE
18b. R_{GAIN} FORCE

WAFER TEST LIMITS at $V_S = \pm 15V$, $R_S = 5k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

			AMP-05GBC	
PARAMETER	**SYMBOL**	**CONDITIONS**	**LIMIT**	**UNITS**
Input Offset Voltage	V_{IOS}	$V_{CM} = 0$	2.0	mV MAX
Output Offset Voltage	V_{OOS}		25	mV MAX
Offset Referred to Input vs. Positive Supply	PSR	V+ = +5V to +15V G = 1000 G = 100 G = 10 G = 1	 110 105 90 70	dB MIN
Offset Referred to Input vs. Negative Supply	PSR	V− = −5V to −15V G = 1000 G = 100 G = 10 G = 1	 105 90 70 50	dB MIN
Input Bias Current	I_B		100	pA MAX
Input Offset Current	I_{OS}		50	pA MAX
Input Voltage Range	IVR	Guaranteed by CMR Tests	±11	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$ G = 1000 G = 100 G = 10 G = 1	 100 95 90 80	dB MIN
Gain Equation Accuracy		$G = 20 \times R_S/R_G$ G = 1 to 100	1.0	% MAX
Output Voltage Swing	V_{OUT}	$R_L = 1k\Omega$	±11	V MIN
Output-Current Limit		Output-to-Ground Short	±20	mA MIN
Current Source	I_{OUT}		90 120	μA MIN μA MAX
Quiescent Current	I_Q		±10.0	mA MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 5k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-05GBC TYPICAL	UNITS
Input Offset Voltage Drift	TCV_{IOS}		7	$\mu V/°C$
Output Offset Voltage Drift	TCV_{OOS}	$R_G = \infty$	70	$\mu V/°C$
Nonlinearity		G = 1000 $R_L = 10k\Omega$	0.004	%
Voltage Noise Density	e_n	G = 1000 $f_O = 1kHz$	16	$nV/\sqrt{Hz}$
Current Noise Density	i_n	G = 1000 $f_O = 1kHz$	10	$fA/\sqrt{Hz}$
Voltage Noise	e_{np-p}	G = 1000 0.1Hz to 10Hz	4	μV_{p-p}
Current Noise	i_{np-p}	G = 1000 0.1Hz to 10Hz	0.12	pA_{p-p}
Small-Signal Bandwidth (−3dB)	BW	G = 1000	120	kHz
Slew Rate	SR	G = 10	7.5	$V/\mu s$
Settling Time	t_S	To 0.025% −10V to +10V Step $1 \le G \le 2000$	10	μs
Overload Recovery Time	t_{rec}	G = 1000 V_{IN} = 10V to 10mV	15	μs

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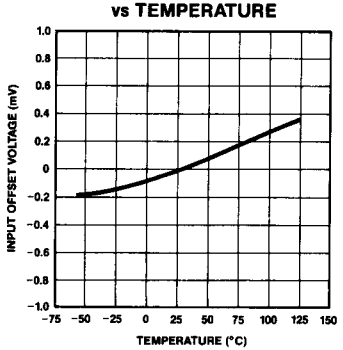
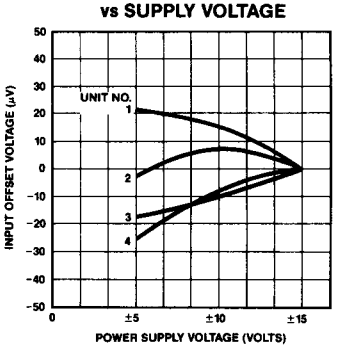
TYPICAL PERFORMANCE CHARACTERISTICS

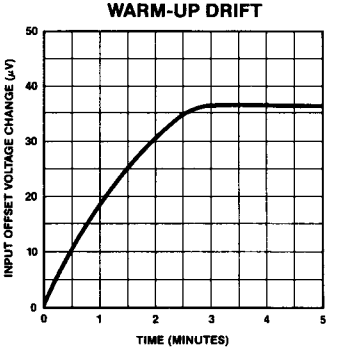
INPUT OFFSET VOLTAGE vs TEMPERATURE



INPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE

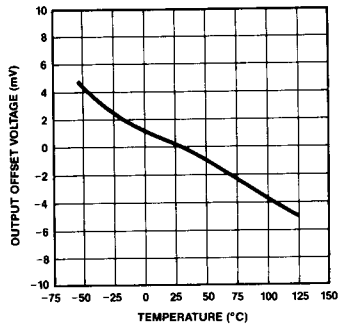


INPUT OFFSET VOLTAGE WARM-UP DRIFT

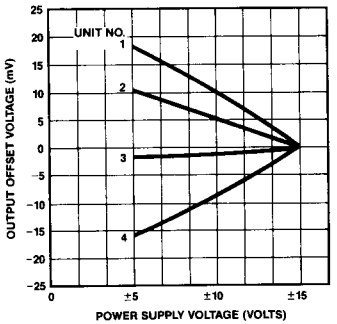


TYPICAL PERFORMANCE CHARACTERISTICS

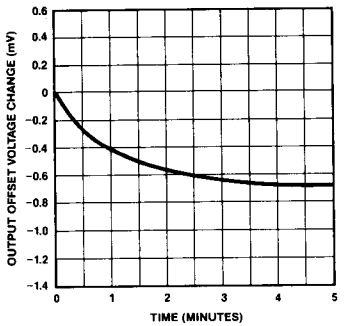
OUTPUT OFFSET VOLTAGE vs TEMPERATURE



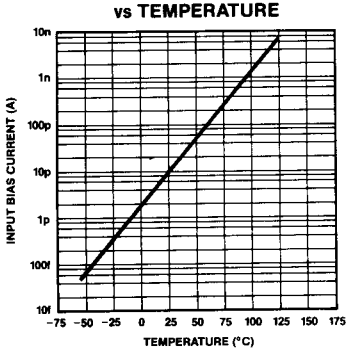
OUTPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE



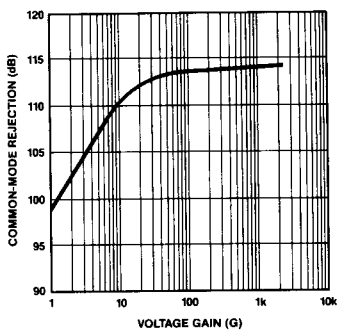
OUTPUT OFFSET VOLTAGE WARM-UP DRIFT



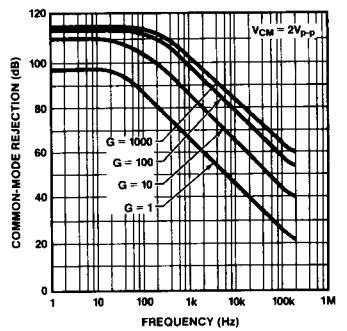
INPUT BIAS CURRENT vs TEMPERATURE



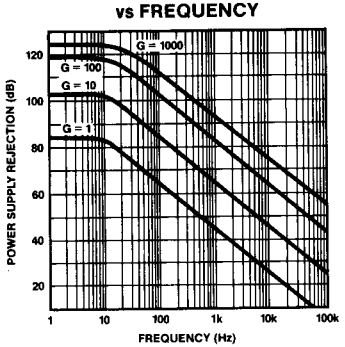
COMMON-MODE REJECTION vs VOLTAGE GAIN



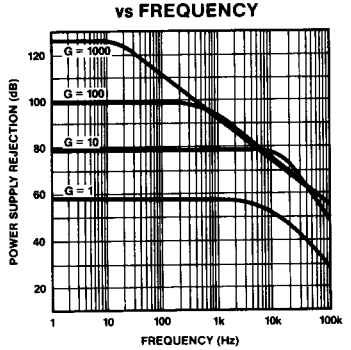
COMMON-MODE REJECTION vs FREQUENCY



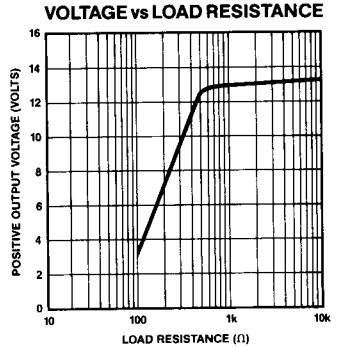
POSITIVE PSR vs FREQUENCY



NEGATIVE PSR vs FREQUENCY

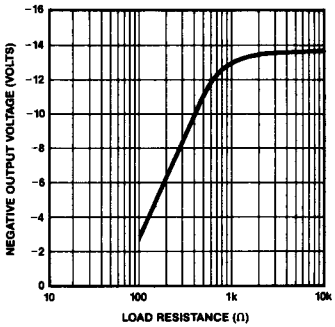


MAXIMUM POSITIVE OUTPUT VOLTAGE vs LOAD RESISTANCE

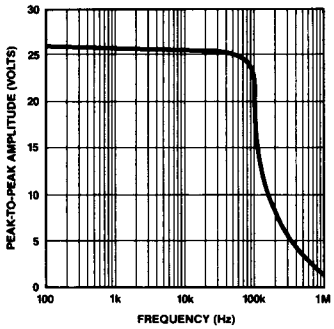


TYPICAL PERFORMANCE CHARACTERISTICS

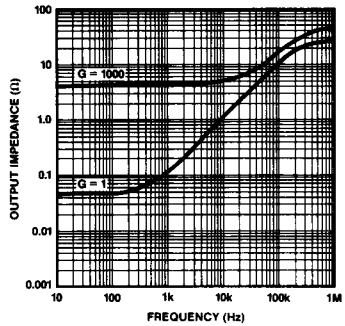
MAXIMUM NEGATIVE OUTPUT VOLTAGE vs LOAD RESISTANCE



MAXIMUM OUTPUT SWING vs FREQUENCY



CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



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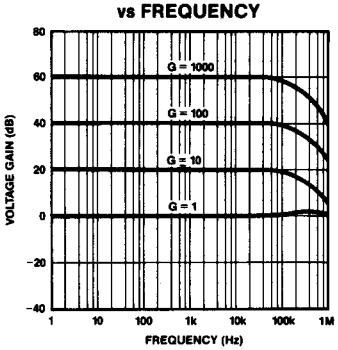
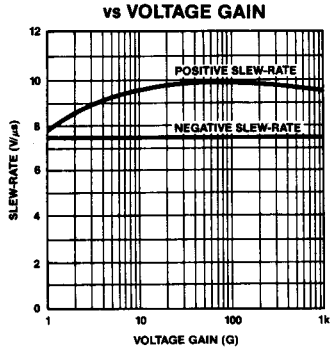
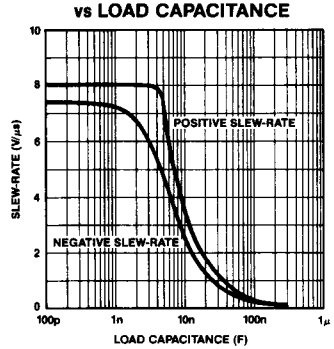
VOLTAGE GAIN vs FREQUENCY



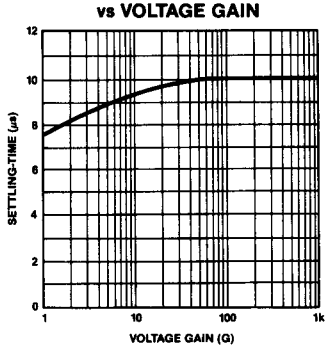
OUTPUT SLEW-RATE vs VOLTAGE GAIN



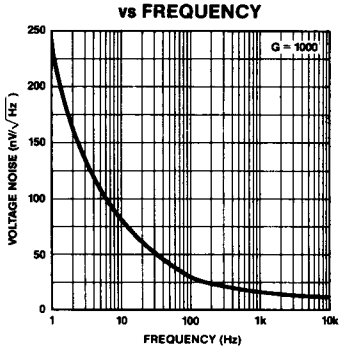
OUTPUT SLEW-RATE vs LOAD CAPACITANCE



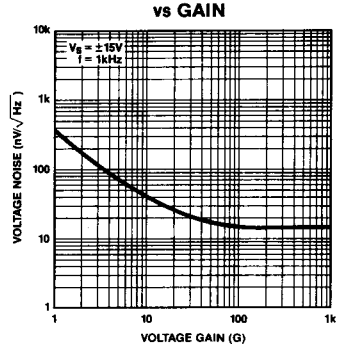
SETTLING-TIME TO 0.025% vs VOLTAGE GAIN



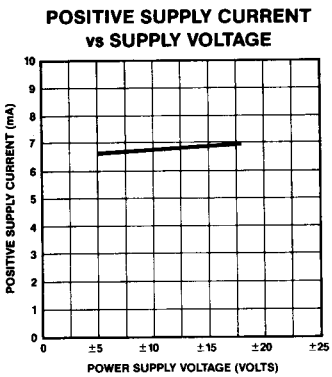
VOLTAGE NOISE DENSITY vs FREQUENCY

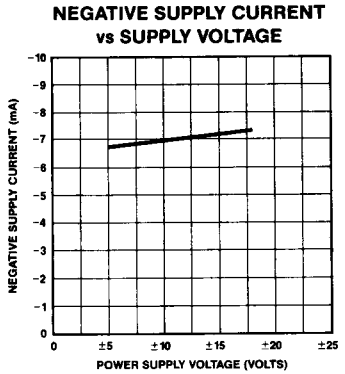


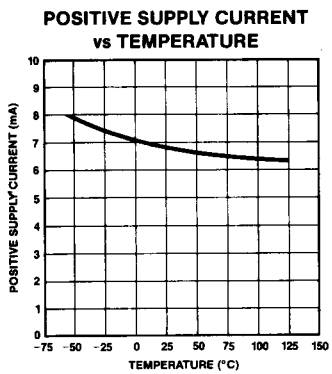
VOLTAGE NOISE DENSITY vs GAIN

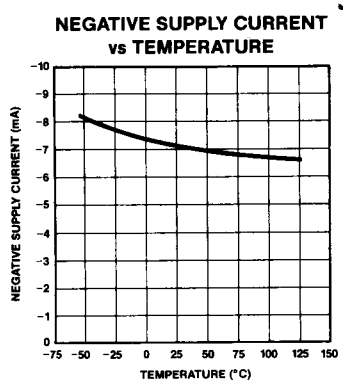


TYPICAL PERFORMANCE CHARACTERISTICS









APPLICATIONS INFORMATION

VOLTAGE GAIN

The AMP-05 uses two external resistors for setting voltage gain over the range 0.1 to 2000. The magnitudes of the scale resistor, R_S, and gain-set resistor, R_G, are related by the formula: $G = 20 \times R_S/R_G$, where G is the selected voltage gain. Figure 1 shows the amplifier connections. R_G can be selected using the graph in Figure 2.

Circuit performance is characterized using $R_S = 5k\Omega$ operating on ±15 volt supplies and driving a ±10 volt output.

Metal-film or wirewound resistors are recommended for R_S and R_G. The absolute resistance values and temperature coefficients of resistance are not too important; only the ratiometric parameters are important for gain accuracy and stability.

FIGURE 1: Basic AMP-05 Connections For Gains 0.1 to 2000

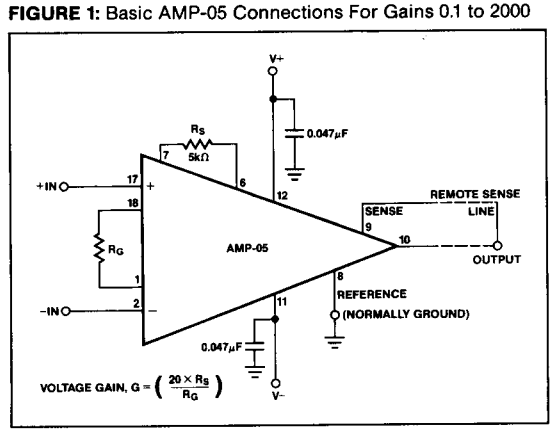
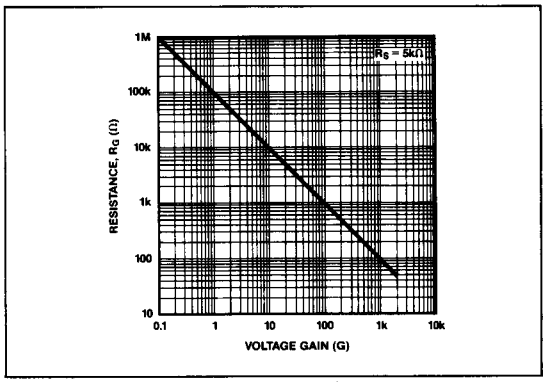


FIGURE 2: Selection of R_{GAIN}



AC amplifiers require good gain stability with temperature and time, but DC performance is unimportant. Therefore, low cost metal-film types with TCs of 50ppm/°C are usually adequate for R_S and R_G. Realizing the full potential of the AMP-05's gain stability requires precision metal-film or wirewound resistors. Achieving a 25ppm/°C max. gain tempco at all gains will require R_S and R_G temperature coefficient matching to 5ppm/°C max.

Gain accuracy is determined by the ratio accuracy of R_S and R_G combined with the gain equation error of the AMP-05 (0.5% for A/E grades).

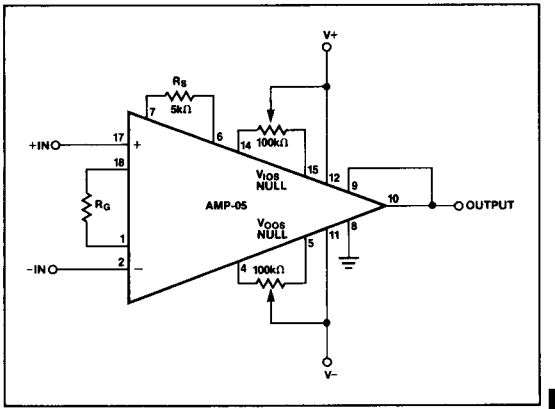
Note: The AMP-05 is inherently stable at all gains. However, like all amplifiers with a high gain-bandwidth product, instability can occur if layout precautions are not observed: (a) the amplifier should be decoupled close to the supply pins, and (b) the output must be kept well away from the inputs, the null pins, and R_{GAIN}.

The AMP-05 is capable of gain-bandwidth products in the hundreds of megahertz when operated at its highest gain settings. Under these conditions, even a few picofarads of stray feedback to the inputs can cause instability, and the situation is exacerbated if the input signal has a high source impedance. If instability does occur, the problem is easily eliminated by placing a small capacitor directly between the AMP-05's input pins, 2 and 17.

INPUT AND OUTPUT OFFSET VOLTAGES

Instrumentation amplifiers have independent offset voltages associated with the input and output stages. While the initial offsets may be adjusted to zero, temperature variations will cause shifts in offsets. Systems with auto-zero can correct for offset errors, so initial adjustment would be unnecessary. However, many high-gain applications do not have auto-zero. For these applications both offsets can be nulled. Nulling has minimal effect on TCV_{IOS} and TCV_{OOS} (refer to Figure 3 for connections).

FIGURE 3: Input and Output Offset Voltage Nulling



The input offset component is directly multiplied by the amplifier gain, whereas output offset is independent of gain. Therefore, at low gain, output offset errors dominate, while at high gain, input offset errors dominate. Overall offset voltage, V_{OS}, referred to the output (RTO) is calculated as follows:

$$V_{OS}\,(RTO) = (V_{IOS} \times G) + V_{OOS} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

where V_{IOS} and V_{OOS} are the input and the output offset voltage specifications and G is the amplifier gain. Input offset nulling alone can be used for fixed gains above 50. Otherwise, both nulls are required. When nulling both initial offsets, the input offset is nulled first by short-circuiting R_G, then the output offset is nulled with the short removed.

The overall offset voltage drift, TCV_{OS}, referred to the output, is a combination of input and output drift specifications. Input offset voltage drift is multiplied by the amplifier gain, G, and summed with the output offset drift;

$$TCV_{OS}\,(RTO) = (TCV_{IOS} \times G) + TCV_{OOS} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

where TCV_{IOS} is the input offset voltage drift, and TCV_{OOS} is the output offset voltage drift specification. Frequently, the amplifier drift is referred back to the input (RTI) which is then equivalent to an input signal change;

$$TCV_{OS}\,(RTI) = TCV_{IOS} + \frac{TCV_{OOS}}{G} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

For example, the maximum input-referred drift of an AMP-05EX set to G = 100 becomes:

$$TCV_{OS}\,(RTI) = 10\mu V/°C + \frac{100\mu V/°C}{100} = 11\mu V/°C \text{ max.}$$

INPUT BIAS AND OFFSET CURRENTS

Input bias currents are additional error sources which can degrade the input signal. Bias currents flowing through the signal source resistance appear as an additional offset voltage. Equal source resistance on both inputs of an instrumentation amplifier will minimize offset changes due to bias current variations with signal voltage and temperature. However, the difference between the two bias currents, the input offset current, produces a nontrimmable error. The magnitude of the error is the offset current times the source resistance.

The AMP-05 has FET inputs which have negligible bias and offset currents at room temperature and consequently can accurately measure signals from high source impedances. However, like all FET devices, the bias current doubles approximately every 10°C increase in junction temperature and therefore bias and offset currents must be carefully considered when operating up to +125°C.

Note: If very high source impedances (~1MΩ) are used and the AMP-05 is used at high gain, then it is recommended that a small capacitor is connected across the inputs to prevent instability.

A current path must always be provided between the differential inputs and analog ground to ensure correct amplifier operation. Floating inputs, such as thermocouples, should be grounded close to the signal source for best common-mode rejection.

OVERVOLTAGE PROTECTION

The AMP-05 features a unique internal protection circuit which permits differential input voltages of up to ±30V even when set for high gain operation. It should be noted however, that the output state during such an overload is not defined. Typically, at gains above 10, severe overloads (≈1000% overrange) will cause the output to sit at about +10V with a low-level oscillation apparent.

Additionally, gross overdriving will cause input currents of up to 100μA to flow in the lower of the two inputs. The increased input current should be borne in mind if interfacing to extremely delicate transducers.

OVERLOAD RECOVERY TIME

Following an input overload, an amplifier takes a finite time to recover, i.e. the amplifier's output has to return to the linear operating region after limiting at one or other supply. The AMP-05 is designed to recover rapidly from input overloads; typically recovery time is 15μs following a 1000:1 overload; voltage gain set to 1000.

Rapid overload recovery is particularly important in a multiplexed data acquisition system using programmable gain. In this application, it is possible for the input to be switched to a high-level signal with gain set high, thus overloading the amplifier. To maintain system speed, it is vital for the amplifier to recover quickly once the overload is removed by reprogramming the gain.

COMMON-MODE REJECTION

Ideally, an instrumentation amplifier responds only to the difference between the two input signals and rejects common-mode voltages and noise. In practice, there is a small change in output voltage when both inputs experience the same common-mode voltage change; the ratio of these voltages is called the common-mode gain. Common-mode rejection (CMR) is the logarithm of the ratio of differential-mode gain to common-mode gain, expressed in dB. CMR specifications are normally measured with a full-range input voltage change and a specified source resistance unbalance.

The current-feedback design used in the AMP-05 inherently yields high common-mode rejection. Unlike resistive feedback designs typified by the three-op-amp IA, the CMR is not degraded by small resistances in series with the reference input. A slight, but trimmable, output offset voltage change results from resistance in series with the reference input.

The common-mode input voltage range, CMVR, for linear operation may be calculated from the formula:

$$CMVR = \pm \left(IVR - \frac{|V_{OUT}|}{2G} \right) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

IVR is the data sheet specification for input voltage range; V_{OUT} is the maximum output signal; and G is the chosen voltage gain. For example, at 25°C, IVR is specified as ±11 volts minimum with ±15 volt supplies. Using a ±10 volt maximum swing output and substituting the figures in (4) simplifies the formula to:

$$CMVR = \pm \left(11 - \frac{5}{G} \right) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (5)$$

For all gains greater than or equal to 5, CMVR is ±10 volt minimum; at gains below 5, CMVR is reduced.

GUARD DRIVERS

Dual guard drivers are included to restore bandwidth, settling-time, and high frequency common-mode rejection (CMR) when shielded cable is used at the input. The guard drivers can handle large capacitive loads and transient currents, but they are not intended for large DC loads. The DC path to ground should be 30kΩ or greater; lower values can upset the AMP-05's internal biasing circuits.

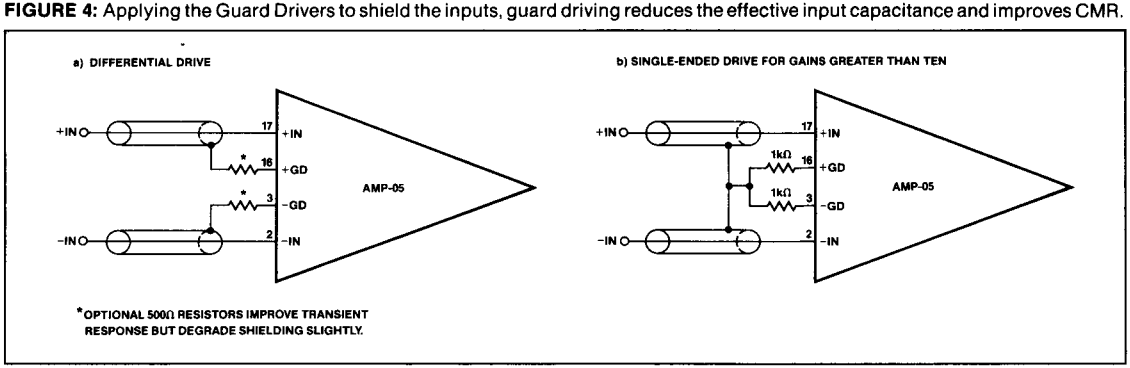
Shielded cable is often employed to minimize capacitively coupled noise pickup along the signal path from source to amplifier. When coaxial cable connects a transducer to the amplifier's input, the cable's capacitance interacts with the transducer's source impedance to form a low-pass filter. This filter function reduces the amplifier's bandwidth and degrades settling-time and CMR. The AMP-05's differential guard drivers act as an AC "bootstrap" when attached to the coaxial shields. In bootstrapping, each driver follows its corresponding input, and the driver output signals are buffered to handle large capacitive loads. Each driver will typically slew at 16V/μs with a 1000pF load. Bootstrapping reduces the effective input capacitance, since no AC voltage appears between the shield and inner conductor.

The AMP-05's guard drivers can form either a differential or single-ended drive (refer to Figures 4(a) and (b)). In the single-ended arrangement, the two input cable shields are held at the same potential, the common-mode voltage (Figure 4(b)). As such, the connection is also appropriate for one shielded twisted-pair cable. The single-ended arrangement maintains a high CMR even at high frequencies, but does not reduce high frequency gain degradation as it does not counteract differential-mode capacitance. Single-ended drive is acceptable for gains greater than ten using the circuit in Figure 4(b). However the differential connection, Figure 4(a), offers better overall performance because it effectively reduces both differential and common-mode capacitance. Reduction in these capacitances improves high-frequency CMR, settling-time, and gain.

It should be noted that all shield drive arrangements are potentially positive feedback configurations and under some conditions high frequency ringing may occur. If this proves troublesome, small resistors (500Ω-1kΩ) in series with the cable shield outputs will improve transient response and settling-time but reduce the effectiveness of the cable shield, particularly at high frequency.

Short circuits from the cable drives to ground will not damage the AMP-05 but will result in malfunction of the AMP-05 until the short is removed. The package pins adjacent to the two inputs, R_G connections and guard drives, sit within 2 volts of the input signals. This feature reduces leakage currents to the input terminals and eliminates the need for guard-rings which are necessary on many FET input amplifiers.

FIGURE 4: Applying the Guard Drivers to shield the inputs, guard driving reduces the effective input capacitance and improves CMR.



GROUNDING

The majority of instruments and data acquisition systems have separate grounds for analog and digital signals. Analog ground may also be divided into two or more grounds which will be tied together at one point, usually the analog power-supply ground. In addition, the digital and analog grounds may be joined, normally at the analog ground pin on the A-to-D converter. Following this basic grounding practice is essential for good circuit performance (Figure 5).

Mixing grounds causes interactions between digital circuits and the analog signals. Since the ground returns have finite resistance and inductance, hundreds of millivolts can be developed between the system ground and the data acquisition components. Using separate ground returns minimizes the current flow in the sensitive analog return path to the system ground point. Consequently, noisy ground currents from logic gates do not interact with the analog signals.

Inevitably, two or more circuits will be joined together with their grounds at differential potentials. In these situations, the differential input of an instrumentation amplifier, with its high CMR, can accurately transfer analog information from one circuit to another.

MAXIMIZING NEGATIVE PSR

Using well stabilized, low-noise power supplies is always recommended for precision analog circuits. However even with good supplies, there will be small changes in output voltage due to temperature variations and line voltage variations. In turn, these voltage changes will affect the amplifier output due to finite power-supply rejection (PSR).

The AMP-05's PSR can be maximized in critical applications by adding a trim potentiometer (see Figure 6). Positive PSR cannot be trimmed by external means but this is better than negative PSR by as much as 20dB, and therefore trimming should not be necessary. Adjusting the negative PSR trim potentiometer also affects output offset voltage, V_{OOS}. Therefore in systems where offset correction is not employed, a V_{OOS} null potentiometer can be added if needed. In practice, the interaction between these two potentiometers is not a problem.

PSR/V_{OOS} trimming procedure: 1) adjust both potentiometers to mid-position; 2) superimpose a low-frequency 1V peak-to-peak sinewave on the negative supply; 3) adjust PSR trim potentiometer for minimum output ripple; 4) remove AC signal from the power supply and null the AMP-05's output offset voltage using the V_{OOS} null potentiometer. Steps 1 and 4 are deleted when only PSR trimming is required.

FIGURE 6: Additional Trim Potentiometer Maximizes Negative PSR

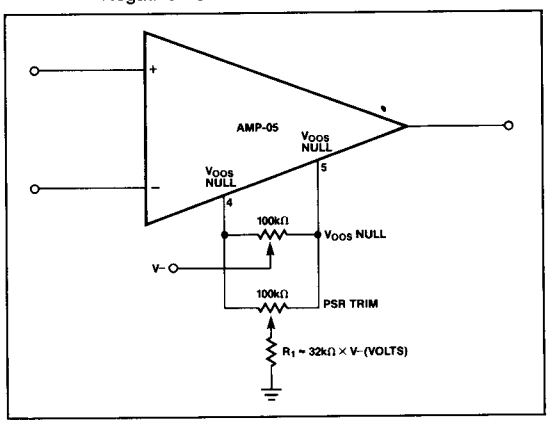
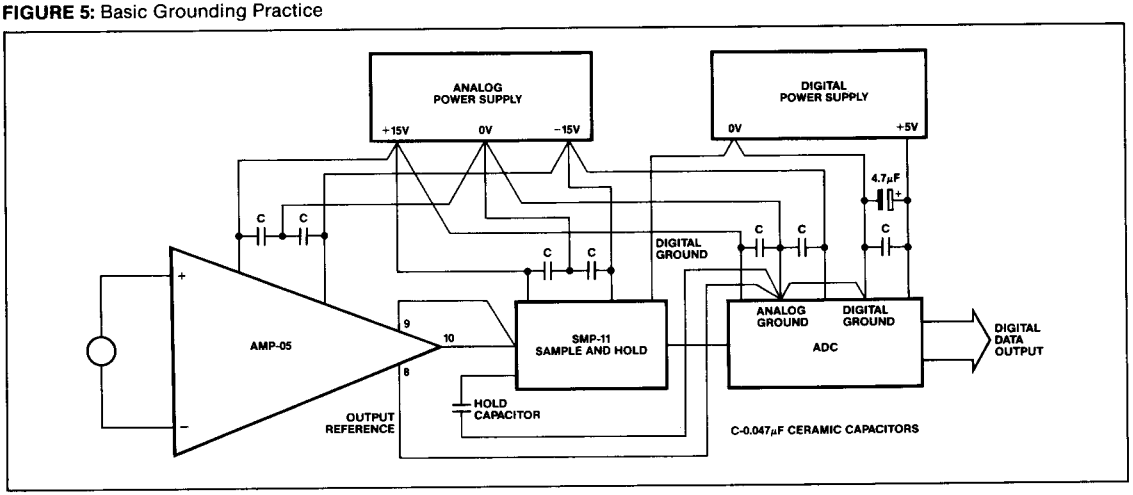


FIGURE 5: Basic Grounding Practice



CURRENT SOURCE

The on-board 100μA current source is provided for transducer excitation, powering a low-current voltage reference diode, and other functions. The current source is referenced from the positive supply rail (V+), and provides a high voltage compliance from 4 to 30V below V+. The output should not be pulled below V−. Output resistance is typically 3GΩ. Simple positive and negative voltage references can be generated by adding two resistors and an inexpensive op amp (Figures 7(a) and (b)). Temperature stability can be improved by replacing R1 with a low-current zener or voltage reference diode such as the LM185. The output reference voltage can be increased beyond the zener voltage by adding resistor R3 to add gain around the OP-77.

If the current source is not used it may be left floating or connected to V−.

SENSE AND REFERENCE TERMINALS

The sense terminal completes the feedback path for the instrumentation amplifier output stage and is normally connected directly to the output. The output signal is specified with respect to the reference terminal, which is normally connected to analog ground.

If high output currents are expected and/or the load is situated some distance from the amplifier, voltage drops due to trace or wire resistance will cause errors. Under these conditions, the sense and reference terminals can be used to "remote sense" the load as shown in Figure 8. This method of connection puts the I × R drops inside the feedback loop and virtually eliminates the error. An unbalance in the lead resistances from the sense and reference pins does not degrade CMR, but will change the output offset voltage. For example, a large unbalance of 3Ω will change the output offset by only 1mV.

FIGURE 7: Generating a Reference Voltage Using the On-Board Current-Source

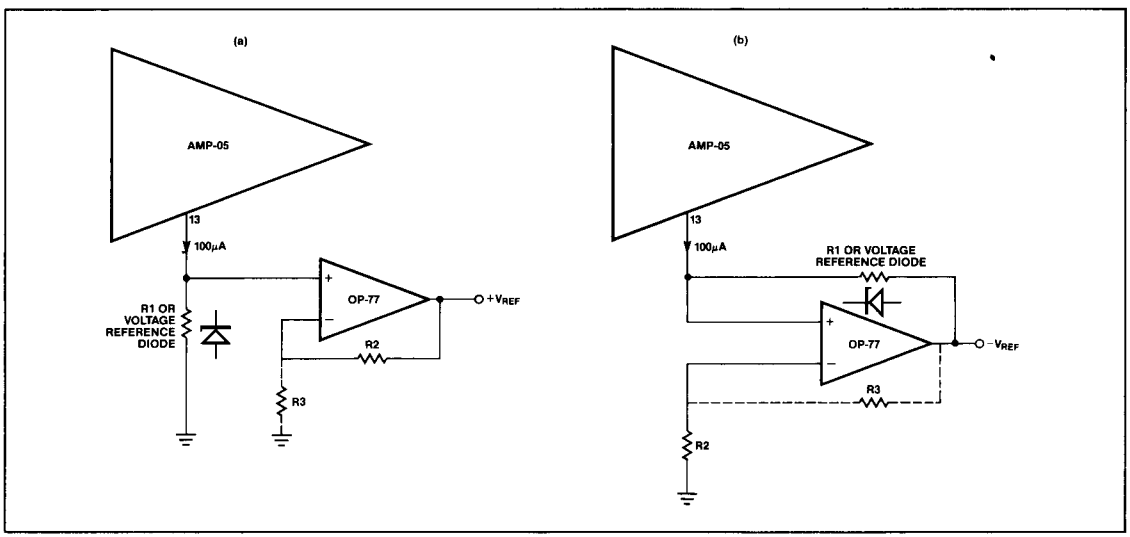
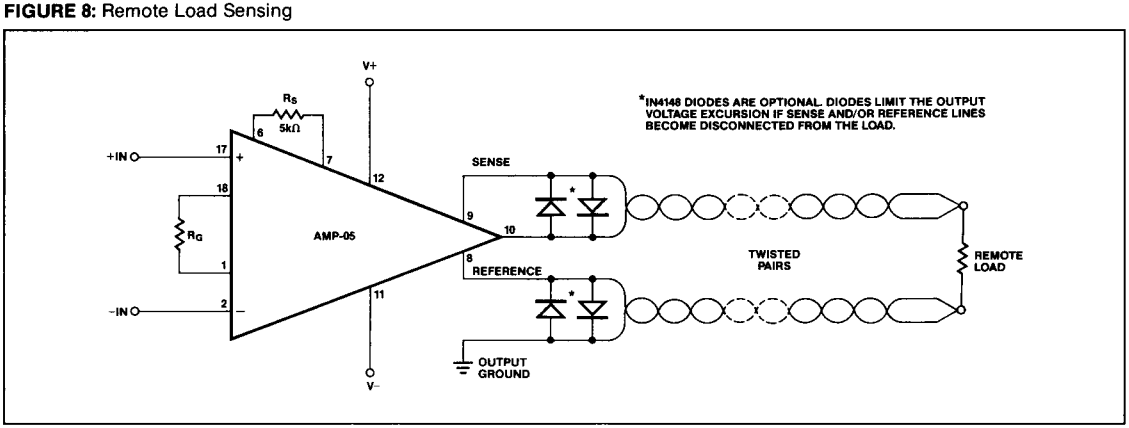


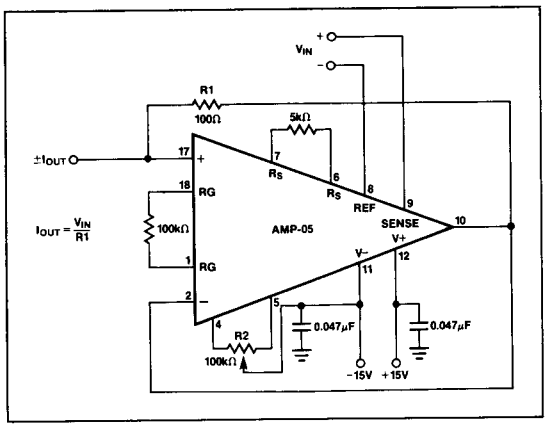
FIGURE 8: Remote Load Sensing



HIGH-COMPLIANCE CURRENT SOURCE

The inputs and outputs of the AMP-05 can be transposed to make a precision bipolar current source (refer to Figure 9). Reference and sense pins become differential inputs and the "old" input now monitors the voltage across a precision current-sense resistor, R1. Voltage gain is set at unity, so the transfer function is simply $I_{OUT} = V_{IN\ (differential)}/R1$. Using a 100Ω resistor for R1 and limiting output current to ±10mA, a reasonable limit for power dissipation reasons, gives a ±1V input requirement for full-scale output. Voltage compliance for ±10mA output is ±10V with a typical output resistance of 50MΩ. Linearity is better than 16-bits at this current level. Potentiometer R2 will trim the output current to zero with the two inputs grounded, and fine gain adjustment is accomplished by trimming R_S or R_G.

FIGURE 9: High-Compliance Current Source With 16-Bit Linearity

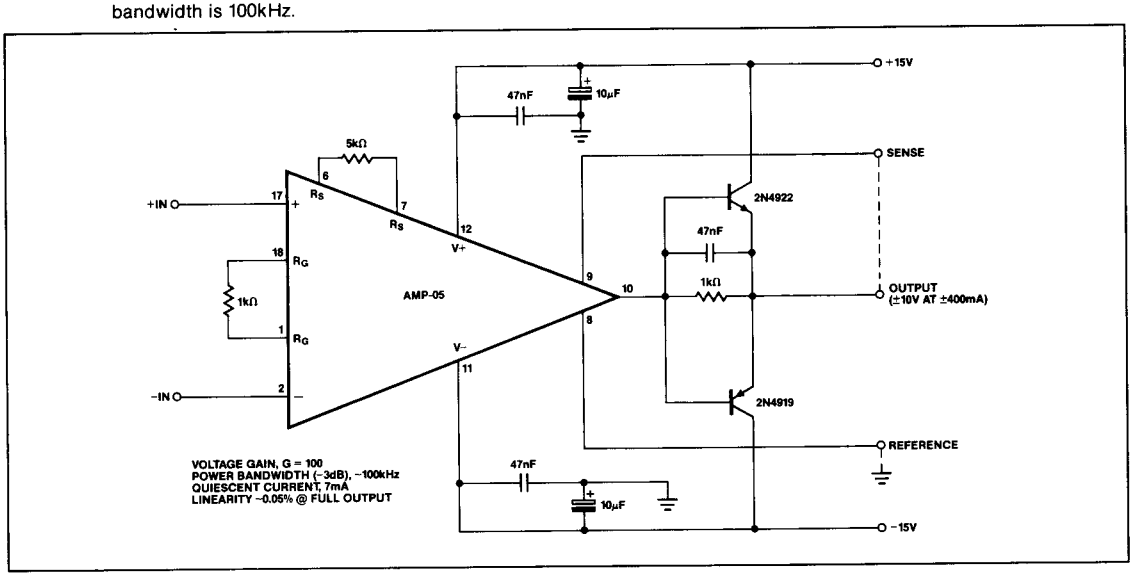


If the class B output stage shown in Figure 10 is added to the basic current-source, then the output current capability is increased to over 100mA with excellent linearity.

SERVO AMPLIFIER

The AMP-05's output power can be boosted by adding a simple class B output stage without increasing the amplifier's quiescent current of 7mA (refer to Figure 10). The 47nF capacitor connected across the transistor's base-emitter junctions prevents instability at V_{OUT} near ground, and reduces high-frequency crossover distortion. DC linearity is typically 0.05% when driving ±10V at ±400mA.

FIGURE 10: Adding two transistors increases output current to ±400mA without affecting the quiescent current of 7mA. Power bandwidth is 100kHz.



ANALOG-MULTIPLEXED DATA ACQUISITION SYSTEMS

For conditioning and digitizing multiple analog signals, there are two traditional system approaches. One dedicates an instrumentation amplifier to condition each input signal, then the high-level outputs are multiplexed and fed to an analog-to-digital converter (ADC). This system is expensive on a "per-channel" basis. A more economical approach is to multiplex unconditioned analog signals and feed them to a programmable-gain instrumentation amplifier, which conditions them before conversion. The per-channel cost drops as the number of channels increases. For this system to have a scan rate comparable to the first, the amplifier's settling-time should be less than the ADC's conversion time. The AMP-05, with its fast settling-time of 15μs maximum to 12 bits, is ideal for this single IA data acquisition system.

A digitally-controlled gain network can easily be added to the AMP-05 as described below.

PROGRAMMABLE-GAIN INSTRUMENTATION AMPLIFIER (PGIA)

Figure 11 shows a programmable gain instrumentation amplifier with digitally selectable gains of 1, 10, 100, and 1000. Each gain set resistor has two MOSFET switches connected back-to-back to prevent all but leakage current from flowing when a switch is OFF. In the high gain positions of 100 and 1000, the calculated values of gain resistor, R_G, are reduced to compensate for the switch ON resistance. The nonlinear switch resistance introduces a slight gain nonlinearity at high gain settings. The PGIA selects gain values in 20μs, including the amplifier settling-time. Gain temperature coefficient depends on R_S, R_G, and on the temperature coefficient of the MOSFET's ON resistance. Values of 15 and 30ppm/°C can be achieved at gains of 1 and 1000, respectively, despite the effect of the high tempco switches.

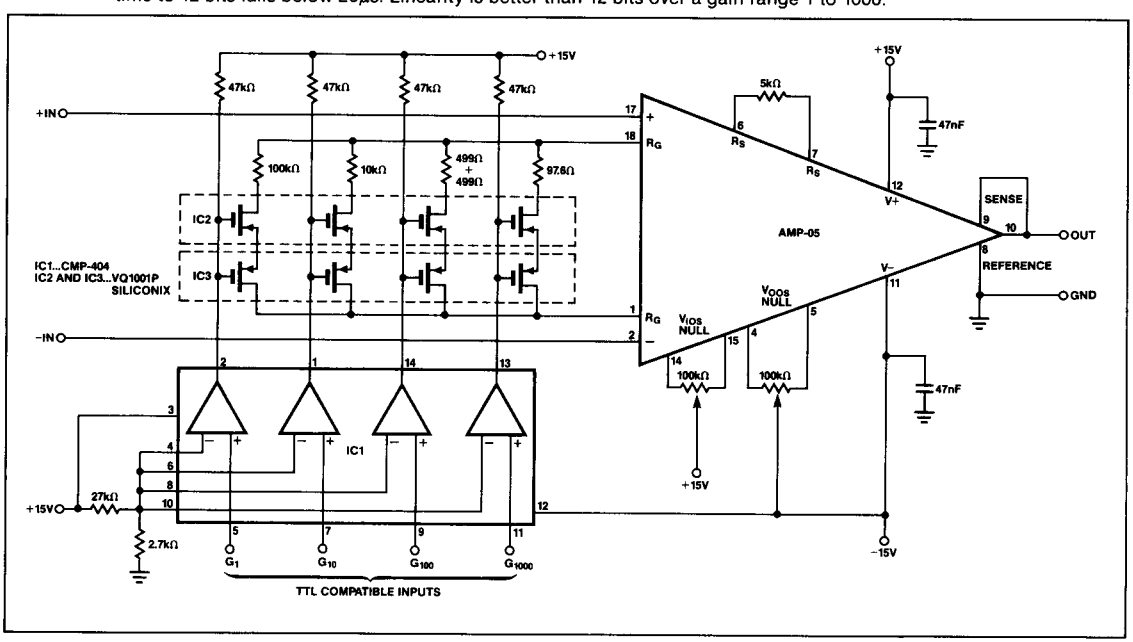
Where fast gain switching is not required, reed relays can substitute for the MOSFET switches. Reed relays have lower ON resistance and OFF leakage current errors. For gains of 100 and 1000, the values of R_G should be increased to 1kΩ and 100Ω respectively, because of lower switch ON resistance. Gain linearity is improved over the original circuit.

AUTO-ZERO SYSTEMS

Offset voltage and drift can be a major error source in high-accuracy systems of 12 bits and above. To minimize initial offset voltage and its associated temperature drift, an auto-zero system can be employed. The technique can potentially keep offset errors well below 1 LSB on a 12-bit system over wide variations in ambient temperature.

For example, consider an instrumentation amplifier set to a gain of 1000 and driving a 12-bit analog-to-digital converter. The input offset voltage drift is 2.5μV/°C, and the output offset voltage drift is negligible. The equivalent output drift is 1000 × 2.5μV/°C, or 2.5mV/°C—more than 1 LSB/°C for a 10V full-scale range. An ambient temperature change from 25°C to 125°C would produce 102 LSBs of drift, excluding the ADC's drift.

FIGURE 11: The AMP-05 makes an excellent programmable-gain instrumentation amplifier. Combined gain-switching and settling-time to 12 bits falls below 20μs. Linearity is better than 12 bits over a gain range 1 to 1000.



Obviously, to limit drift to 1 LSB or less over temperature demands some means of offset correction. Usually both hardware and software are employed to generate an error correction signal which is fed into the reference input of the instrumentation amplifier. Software alone could remove the system's offset error, but at the expense of the full-scale range for very large errors. Part of a typical auto-zero system is shown in Figure 12.

The sequence of events for auto-zeroing a system starts with switching the multiplexer so that the amplifier's two inputs are grounded. The amplifier is given time to settle, and the ADC (not shown) digitizes any system offset. The computer reads the offset and feeds a digital correction to the digital-to-analog converter. To verify that the offset is nulled, a second conversion may be performed, and the multiplexer then switches to measure the input signal.

For a system with a digitally programmable gain, the auto-zeroing process should be repeated for each gain setting. Each correction value can be stored in memory and recalled and refreshed as needed to correct for system drift with time and temperature.

SETTLING-TIME MEASUREMENT

Figure 13 is the test circuit used to measure settling-time. The circuit technique is similar to the "false sum-node" technique used to measure op amp settling-time. For simplicity, the connections for input and output offset nulling are not shown on the circuit, but null pots are required. Measurement set-up:

1. Set switches to G = 1, ground V_{IN}, and short-circuit R_G.
2. Adjust V_{IOS} null pot for minimum output voltage on pin 10.
3. Remove short-circuit from R_G and adjust V_{OOS} null pot for minimum output voltage on pin 10.
4. Apply a low frequency (~100Hz) $20V_{p-p}$ square-wave to V_{IN} and adjust 200Ω pot for minimum square-wave on V_{OUT}.
5. Increase square-wave input frequency and monitor V_{OUT} with an oscilloscope. Settling-time to a 0.025% error band for a 20V input step is measured with limits of ±2.5mV at V_{OUT}.
6. Change switch gain-positions and repeat settling-time measurements for G = 10, 100, and 1000.

FIGURE 12: Instrumentation Amplifier with Offset Correction System

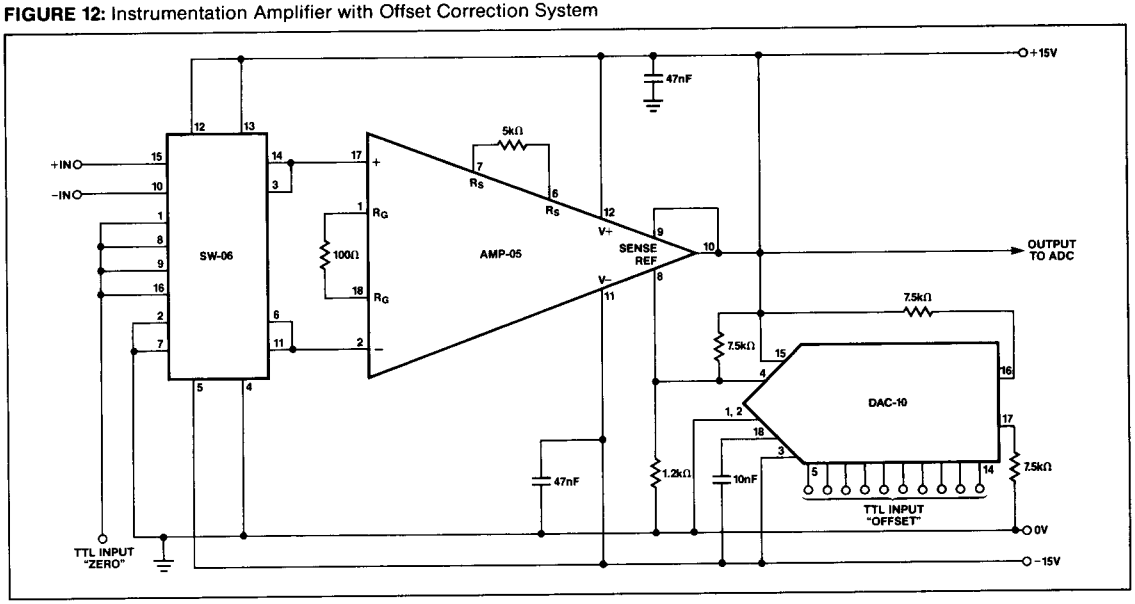


FIGURE 13: Settling-Time Test Circuit

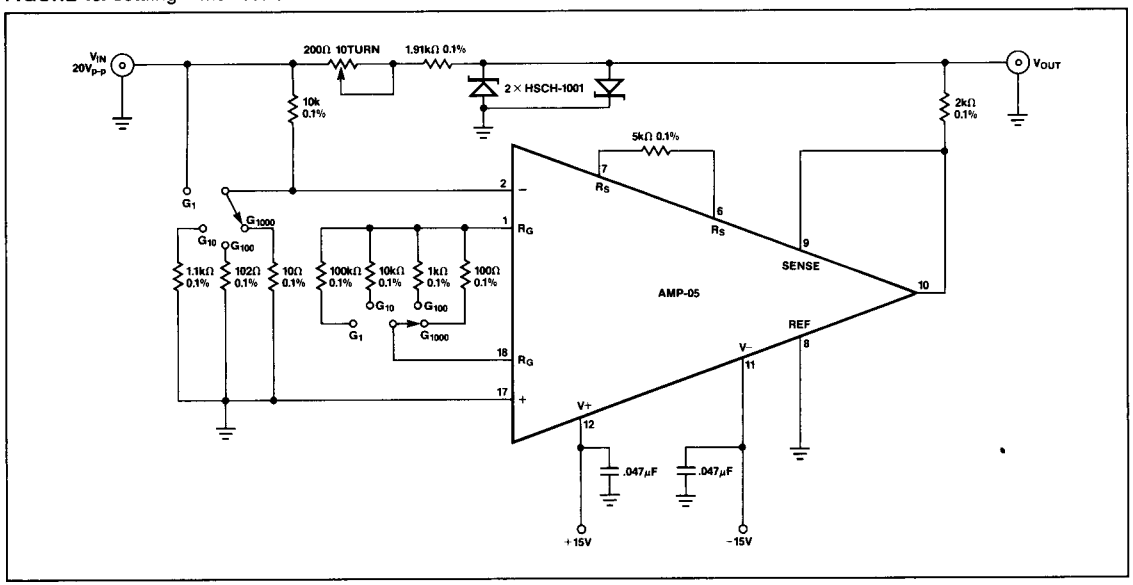


FIGURE 14: Burn-In Circuit