# CMOS Monolithic 256×18 Color Palette RAM-DAC

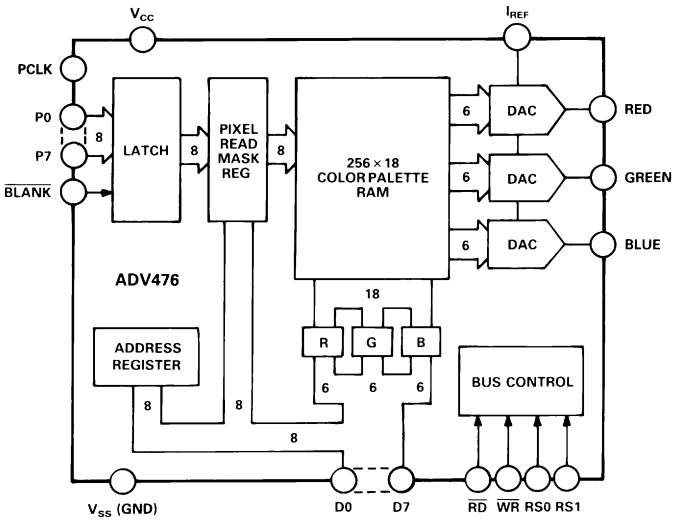
# ADV476

**FEATURES**
**Personal System/2* and VGA* Compatible**
**Plug-in Replacement for INMOS 171/176**
**66 MHz Pipelined Operation**
**Three 6-Bit D/A Converters**
**256×18 Color Palette RAM**
**RS-343A/RS-170 Compatible Outputs**
**Blank on All Three Channels**
**Standard MPU Interface**
**Asynchronous Access to All Internal Registers**
**+5 V CMOS Monolithic Construction**
**Low Power Dissipation**
**Standard 28-Pin, 0.6" DIP and 44-Pin PLCC**

**APPLICATIONS**
**High Resolution Color Graphics**
**CAE/CAD/CAM Applications**
**Image Processing**
**Instrumentation**
**Desktop Publishing**

**AVAILABLE CLOCK RATES**
**66 MHz**
**50 MHz**
**35 MHz**

**FUNCTIONAL BLOCK DIAGRAM**




**GENERAL DESCRIPTION**

The ADV476 (ADV®) is a pin compatible and software compatible RAM-DAC designed specifically for VGA and Personal System/2 color graphics.

The ADV476 is a complete analog output RAM-DAC on a single monolithic chip. The part contains a 256×18 color lookup table, a pixel mask register as well as a triple 6-bit video D/A converter. The ADV476 is capable of simultaneously displaying up to 256 colors, from a total color palette of 262,144 addressable colors.

The on-chip asynchronous MPU bus allows access to the color lookup table without affecting the input video data via the pixel port. The pixel read mask register provides a convenient way of altering the displayed colors without updating the color lookup table. The ADV476 is capable of generating RGB video output signals which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

The ADV476 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation and small board area. The part is packaged in a 0.6", 28-pin DIP and a 44-pin PLCC.

**PRODUCT HIGHLIGHTS**

1. Standard video refresh rates, 35 MHz, 50 MHz and 66 MHz.
2. Fully compatible with VGA and Personal System/2 color graphics.
3. Guaranteed monotonic. Integral and differential linearity guaranteed to be a maximum of ±1 LSB.
4. Low glitch energy, 75 pV secs.

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**ADV is a registered trademark of Analog Devices, Inc.**

REV. B



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# ADV476–SPECIFICATIONS ($V_{CC}$ = +5 V ± 10%, $I_{REF}$ = 8.88 mA. All Specifications $T_{MIN}$ to $T_{MAX}$[1] unless otherwise noted.)

| Parameter | All Versions | Units | Test Conditions/Comments |
|---|---|---|---|
| STATIC PERFORMANCE | | | |
| Resolution (Each DAC) | 6 | Bits | |
| Accuracy (Each DAC) | | | |
| Integral Nonlinearity | ±0.5 | LSB max | Guaranteed Monotonic |
| Full Scale Error | ±5 | % max | Full Scale = 2.15 × $I_{REF}$ × $R_L$, $I_{REF}$ = 8.39 mA |
| Blank Level | ±0.5 | LSB max | $\overline{BLANK}$ = Logic Low |
| Offset Error | ±0.5 | LSB max | $\overline{BLANK}$ = Logic High |
| DIGITAL INPUTS | | | |
| Input High Voltage, $V_{INH}$ | 2 | V min | |
| Input Low Voltage, $V_{INL}$ | 0.8 | V max | |
| Input Current, $I_{IN}$ | ±10 | µA max | $V_{CC}$ = 5.5 V, $V_{IN}$ = 0.4 V to $V_{CC}$ |
| Input Current ($\overline{RD}$ Input Only) | ±100 | µA max | $V_{CC}$ = 5.5 V, $V_{IN}$ = 0.4 V to $V_{CC}$ |
| Input Capacitance, $C_{IN}$ | 7 | pF typ | |
| DIGITAL OUTPUTS | | | |
| Output High Voltage, $V_{OH}$ | 2.4 | V min | $I_{SOURCE}$ = 500 µA, $V_{CC}$ = 4.5 V |
| Output Low Voltage, $V_{OL}$ | 0.4 | V max | $I_{SINK}$ = 5.0 mA, $V_{CC}$ = 4.5 V |
| Floating-State Leakage Current | ±50 | µA max | $V_{CC}$ = 5.5 V, 0.4 V < $V_{IN}$ < $V_{CC}$ |
| Floating-State Output Capacitance | 7 | pF typ | |
| ANALOG OUTPUTS | | | |
| Max Output Voltage | 1.5 | V min | IO < 10 mA, IO = 2.15 × $I_{REF}$ |
| Max Output Current | 21 | mA min | VO ≤ 1 V |
| DAC to DAC Matching[2] | ±2.5 | % max | |
| Analog Output Capacitance | 10 | pF typ | $\overline{BLANK}$ = Logic Low |
| CURRENT REFERENCE | | | |
| Input Current ($I_{REF}$) Range | –3/–10 | mA min/mA max | |
| Voltage at $I_{REF}$ | $V_{CC}$ –3/$V_{CC}$ | V min/V max | $I_{REF}$ = 8.88 mA |
| POWER SUPPLY | | | |
| Supply Voltage, $V_{CC}$ | 4.5/5.5 | V min/V max | |
| Supply Current, $I_{CC}$ | 220 | mA max | $f_{MAX}$ = 66 MHz IO = 2.15 × $I_{REF}$, D0–D7 Unloaded |
| Power Supply Rejection Ratio | 6 | %/V | 4.5 < $V_{CC}$ < 5.5 V, IO = 2.15 × $I_{REF}$, $R_L$ = 37.5 Ω, $C_L$ = 30 pF, $I_{REF}$ = 8.88 mA. |
| DYNAMIC PERFORMANCE | | | |
| Clock and Data Feedthrough[3, 4] | –35 | dB typ | |
| Glitch Impulse[3, 4] | 75 | pV secs typ | |

NOTES

[1]Temperature range ($T_{MIN}$ to $T_{MAX}$); 0 to +70°C.

[2]Relative to the midpoint of the distribution of the three DACs measured at full scale.

[3]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10 pF, 37.5 Ω. D0–D7 output load ≤50 pF. See timing notes in Figure 2.

[4]Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2 × clock rate.

Specifications subject to change without notice.

# TIMING CHARACTERISTICS[1] ($V_{CC}$ = +5 V ± 10%. All Specifications $T_{MIN}$ to $T_{MAX}$[2])

| Parameter | 66 MHz Version | 50 MHz Version | 35 MHz Version | Units | Conditions/Comments |
|---|---|---|---|---|---|
| $f_{MAX}$ | 66 | 50 | 35 | MHz | Clock Rate |
| $t_1$ | 10 | 10 | 15 | ns min | RS0, RS1 Setup Time |
| $t_2$ | 10 | 10 | 15 | ns min | RS0, RS1 Hold Time |
| $t_3$ | 5 | 5 | 5 | ns min | $\overline{RD}$ Asserted to Data Bus Driven |
| $t_4$ | 40 | 40 | 40 | ns max | $\overline{RD}$ Asserted to Data Valid |
| $t_5$ | 20 | 20 | 20 | ns max | $\overline{RD}$ Negated to Data Bus 3-Stated |
| $t_6$ | 10 | 10 | 15 | ns min | Write Data Setup Time |
| $t_7$ | 10 | 10 | 15 | ns min | Write Data Hold Time |
| $t_8$ | 50 | 50 | 50 | ns min | $\overline{RD}$, $\overline{WR}$ Pulse Width Low |
| $t_9$ | $4\times t_{12}$ | $4\times t_{12}$ | $4\times t_{12}$ | ns min | $\overline{RD}$, $\overline{WR}$ Pulse Width High |
| $t_{10}$ | 3 | 3 | 4 | ns min | Pixel & Control Setup Time |
| $t_{11}$ | 3 | 3 | 4 | ns min | Pixel & Control Hold Time |
| $t_{12}$ | 15.3 | 20 | 28 | ns min | Clock Cycle Time |
| $t_{13}$ | 5 | 6 | 7 | ns min | Clock Pulse Width High Time |
| $t_{14}$ | 5 | 6 | 9 | ns min | Clock Pulse Width Low Time |
| $t_{15}$ | 30 | 30 | 30 | ns max | Analog Output Delay |
| | 5 | 5 | 5 | ns min | |
| $t_{16}$ | 6 | 8 | 8 | ns max | Analog Output Rise/Fall Time |
| $t_{17}$[3] | 15.3 | 20 | 25 | ns typ | Analog Output Settling Time |
| $t_{18}$ | 2 | 2 | 2 | ns min | Analog Output Skew |
| $t_{PD}$ | 4 | 4 | 4 | clocks | Pipeline Delay |

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10 pF, 37.5 Ω. D0–D7 output load ≤50 pF. See timing notes in Figure 2.
[2]Temperature Range ($T_{MIN}$ to $T_{MAX}$); 0 to +70°C
[3]Settling time does not include clock and data feedthrough. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic.

Specifications subject to change without notice.

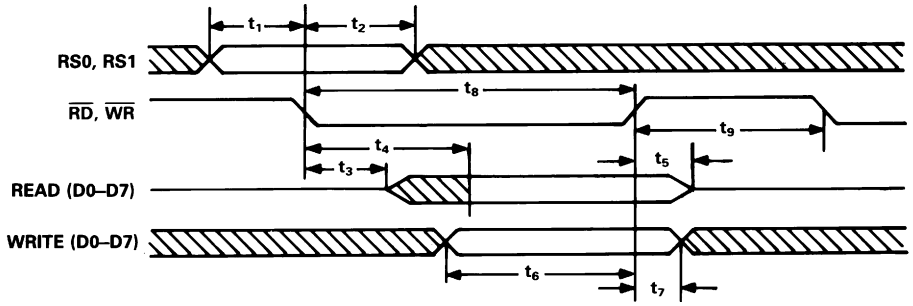
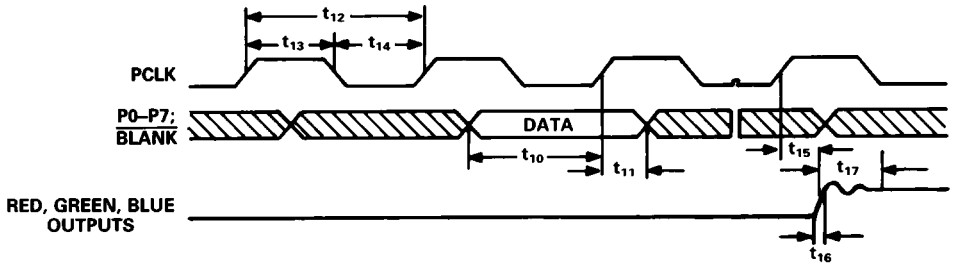



*Figure 1. MPU Read/Write Timing*




**NOTES**
**1. OUTPUT DELAY ($t_{15}$) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF THE PCLK TO THE 50% POINT OF FULL SCALE TRANSITION.**
**2. SETTLING TIME ($t_{17}$) MEASURED FROM THE 50% POINT OF FULL SCALE TRANSITION TO THE OUTPUT REMAINING WITHIN ±1/4 LSB.**
**3. OUTPUT RISE/FALL TIME ($t_{16}$) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL SCALE TRANSITION.**

*Figure 2. Video Input/Output Timing*

**ABSOLUTE MAXIMUM RATINGS**[1]

$V_{CC}$ to GND ..... +7 V
Voltage on any Digital Pin ..... GND – 0.5 V to $V_{CC}$ + 0.5 V
Ambient Operating Temperature ($T_A$) ..... –55°C to +125°C
Storage Temperature ($T_S$) ..... –65°C to +150°C
Junction Temperature ($T_J$) ..... +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
Vapor Phase Soldering (1 minute) ..... +220°C
Red, Green, Blue to GND[2] ..... 0 V to $V_{CC}$

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Analog output short circuit to any power supply or common can be of an indefinite duration.

**ORDERING GUIDE**[1, 2]

| Model | Speed | Package Type | Package Option[3] |
|---|---|---|---|
| ADV476KN35 | 35 MHz | 28-Pin DIP | N-28 |
| ADV476KN50 | 50 MHz | 28-Pin DIP | N-28 |
| ADV476KN66 | 66 MHz | 28-Pin DIP | N-28 |
| ADV476KP35 | 35 MHz | 44-Pin PLCC | P-44A |
| ADV476KP50 | 50 MHz | 44-Pin PLCC | P-44A |
| ADV476KP66 | 66 MHz | 44-Pin PLCC | P-44A |

NOTES
[1]All devices are specified for 0°C to +70°C operation.
[2]Devices are packaged in 0.6" 28-pin plastic DIPs (N-28), and 44-pin J-leaded PLCC (P-44A).
[3]N = Plastic DIP; P = Plastic Leaded Chip Carrier.

**RECOMMENDED OPERATING CONDITIONS**

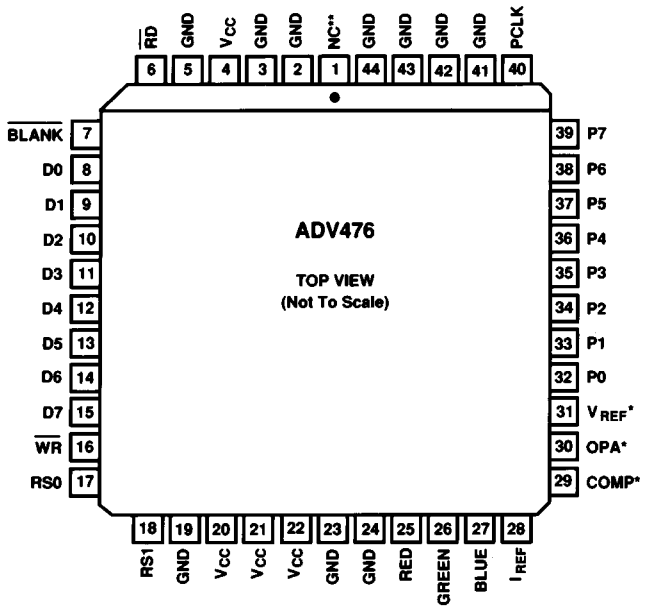
| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Power Supply | $V_{CC}$ | 4.5 | 5.00 | 5.5 | Volts |
| Ambient Operating Temperature | $T_A$ | 0 | | +70 | °C |
| Output Load | $R_L$ | | 37.5 | | Ω |
| Reference Current | $I_{REF}$ | –3 | | –10 | mA |

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV476 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

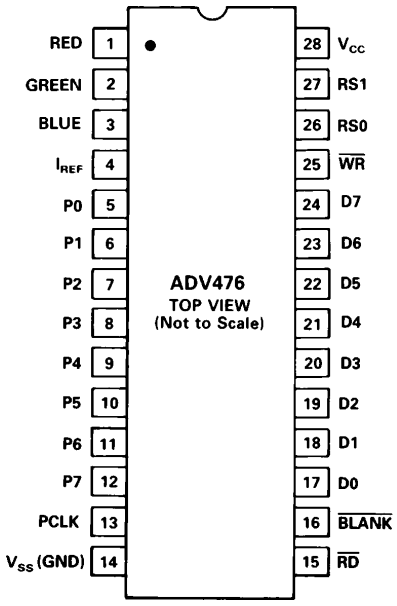

**PIN CONFIGURATIONS**

**PLCC**




*$V_{REF}$ MUST BE TERMINATED THROUGH A 0.1μF CERAMIC CAPACITOR TO $V_{CC}$ OPA IS LEFT UNCONNECTED; COMP IS CONNECTED TO $I_{REF}$ (SEE FIGURE 8).
**NC = NO CONNECT

**DIP**




The above pins allow the ADV476KP (44-Pin PLCC) to be alternatively driven by a voltage reference. If it is desired to use a voltage reference configuration instead of the current reference configuration described in this data sheet, the above listed pins must be connected as described in Figure 6 of the ADV478/ADV471 data sheet of this reference manual.

**PIN FUNCTION DESCRIPTION**

| Pin Mnemonic | Function |
|---|---|
| $\overline{\text{BLANK}}$ | Composite blank control input (TTL compatible). A logic zero on this control input drives the analog outputs to the blanking level, as shown in Table V. The $\overline{\text{BLANK}}$ signal is latched on the rising edge of PCLK. While $\overline{\text{BLANK}}$ is a logical zero, the pixel inputs are ignored. |
| PCLK | Clock input (TTL compatible). The rising edge of PCLK latches the P0–P7 data inputs and the $\overline{\text{BLANK}}$ control input. It is typically the pixel clock rate of the video system. PCLK should be driven by a dedicated TTL buffer. |
| P0–P7 | Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. P0–P7 pixel select inputs are latched on the rising edge of PCLK. P0 is the LSB. Unused pixel select inputs should be connected to GND. |
| RED, GREEN, BLUE | Red, green and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable, as shown in Figure 4a. All three current outputs should have similar output loads whether or not they are all being used. |
| $V_{CC}$ | Analog power supply (5 V ± 10%). |
| GND | Analog ground. |
| $I_{REF}$ | Current reference input. The relationship between the current input and the full scale output voltage of the DACs is given by the following expression:<br>$I_{REF}$ = VO (Full Scale)/2.15 × $R_L$<br>$R_L$ = Load Resistance |
| $\overline{\text{WR}}$ | Write control input (TTL compatible). $\overline{\text{WR}}$ must be at logical zero when writing data to the device. D0–D7 data is latched on the rising edge of $\overline{\text{WR}}$. See Figure 1. |
| $\overline{\text{RD}}$ | Read control input (TTL compatible). $\overline{\text{RD}}$ must both be at logical zero when reading data from the device. See Figure 1. |
| RS0, RS1 | Command control inputs (TTL compatible). RS0 and RS1 specify the type of read or write operation being carried out, i.e., address register or color palette RAM read or write operations. See Tables I, II, III. |
| D0–D7 | Data bus (TTL compatible). Data is transferred to and from the address register and the color palette RAM over this 8-bit bidirectional data bus. D0 is the least significant bit. |

**TERMINOLOGY**

**Blanking Level**
The level separating the SYNC portion from the Video portion of the waveform. Usually referred to as the Front Porch or Back Porch. At 0 IRE Units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

**Color Video (RGB)**
This usually refers to the technique of combining the three primary colors of Red, Green and Blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs are required, one for each color.

**Gray Scale**
The discrete levels of video signal between Reference Black and Reference White levels. An 8-bit DAC contains 256 different levels while a 6-bit DAC contains 64.

**Raster Scan**
The most basic method of sweeping a CRT one line at a time to generate and display images.

**Reference Black Level**
The maximum negative polarity amplitude of the video signal.

**Reference White Level**
The maximum positive polarity amplitude of the video signal.

**Video Signal**
That portion of the composite video signal which varies in gray scale levels between Reference White and Reference Black. Also referred to as the picture signal, this is the portion which may be visually observed.

**MPU Interface**

As illustrated in the functional block diagram, the ADV476 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM.

The RS0 and RS1 control inputs specify whether the MPU is accessing the address register or the color palette RAM, as shown in Table I. The 8-bit address register is used to address the color palette RAM, eliminating the requirement for external address multiplexers.

**Table I. Control Input Truth Table**

| RS1 | RS0 | Addressed by MPU |
|---|---|---|
| 0 | 0 | Pixel Address Register (RAM Write Mode) |
| 1 | 1 | Pixel Address Register (RAM Read Mode) |
| 0 | 1 | Color Palette RAM |
| 1 | 0 | Pixel Read Mask Register |

To write color data, the MPU writes to the address register with the 8-bit address of the color palette RAM location which is to be modified. The MPU performs three successive write cycles (six bits of red data, six bits of green data and six bits of blue data). During the blue write cycle, the three bytes of color information are concatenated into an 18-bit word and written to the location specified by the address register. The address register then automatically increments to the next location which the MPU may modify by simply writing another sequence of red, green and blue data.

To read back color data, the MPU loads the address register with the address of the color palette RAM location to be read. The MPU performs three successive read cycles (6 bits each of red, green and blue data). Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequence of red, green and blue data.

This 6-bit color data is right justified, i.e., the lower six bits of the data bus with D0 being the LSB and D5 the MSB. D6 and D7 are ignored during a color write cycle and are set to zero during a color read cycle.

During color palette RAM access, the address register resets to 00H following a blue read or write operation to RAM location FFH.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. Color (RGB) data is normally loaded to the color palette RAM during video screen retrace, i.e., during the video waveform blanking period, see Figure 5.

To keep track of the red, green and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table II. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle, (ADDR0–7) are accessible to the MPU, and are used to address color palette RAM locations, as shown in Table III. ADDR0 is the LSB when the MPU is accessing the RAM. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Figure 1 illustrates the MPU read/write timing and Table III shows the associated functional instructions.

**Table II. Address Register (ADDR) Operation**

| | Value | RS1 | RS0 | Addressed by MPU |
|---|---|---|---|---|
| ADDRa,b (Counts Modulo 3) | 00<br>01<br>10 | | | Red Value<br>Green Value<br>Blue Value |
| ADDR0–7 (Counts Binary) | 00H–FFH | 0 | 1 | Color Palette RAM |

**Table III. Truth Table for Read/Write Operations**

| $\overline{RD}$ | $\overline{WR}$ | RS0 | RS1 | ADDRa | ADDRb | Operation Performed | |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | X | X | Write Address Register; | D0–D7→ADDR0–7<br>0→ADDRa,b |
| 1 | 0 | 1 | 0 | 0 | 0 | Write Red Value; | Increment ADDRa–b |
| 1 | 0 | 1 | 0 | 0 | 1 | Write Green Value; | Increment ADDRa–b |
| 1 | 0 | 1 | 0 | 1 | 0 | Write Blue Value; | Modify RAM Location<br>Increment ADDR0–7<br>Increment ADDRa–b |
| 0 | 1 | 1 | 1 | X | X | Read Address Register; | ADDR0–7→D0–D7 |
| 0 | 1 | 1 | 0 | 0 | 0 | Read Red Value; | Increment ADDRa–b |
| 0 | 1 | 1 | 0 | 0 | 1 | Read Green Value; | Increment ADDRa–b |
| 0 | 1 | 1 | 0 | 1 | 0 | Read Blue Value; | Increment ADDR0–7<br>Increment ADDRa–b |
| 0 | 0 | X | X | X | X | Invalid Operation | |

**Frame Buffer Interface**

The P0-P7 inputs are used to address the color palette RAM, as shown in Table IV. These inputs are latched on the rising edge of PCLK and address any of the 256 locations in the color palette RAM. The addressed location contains 18 bits of color (6 bits of red, 6 bits of green and 6 bits of blue) information. This data is transferred to the three DACs and is then converted to an analog output (RED, GREEN, BLUE), these outputs then control the red, green and blue electron guns in the monitor.

The $\overline{\text{BLANK}}$ input is also latched on the rising edge of PCLK. This is to maintain synchronization with the color data.

**Table IV. Pixel Select/Color Palette Control Truth Table**

| P0–P7 | Addressed by Frame Buffer |
|---|---|
| 00H | Color Palette RAM Location 00H |
| 01H | Color Palette RAM Location 01H |
| • | • • |
| • | • • |
| FFH | Color Palette RAM Location FFH |

**Pixel Read Mask Register**

The Pixel Read Mask Register in the ADV476 can be used to implement register level pixel processing, thereby cutting down on software overhead. This is achieved by gating the input pixel stream (P0–P7) with the contents of the pixel read mask register. The operation is a bitwise logical ANDing of the pixel data. The contents of This register can be accessed and altered at any time by the MPU (D0–D7). Table I shows the relevant control signals.

This pixel masking operation can be used to alter the displayed colors without changing the contents of either the video frame buffer or the color palette RAM. The effect of this operation is to partition the color palette into a user determined number of color planes. This process can be used for special effects including animation, overlays and flashing objects.

(See also application note entitled "Animation Using the Pixel Read Mask Register of the ADV47x Series of Video RAM-DACs," available from Analog Devices (Pub No. E1316–15–10/89).

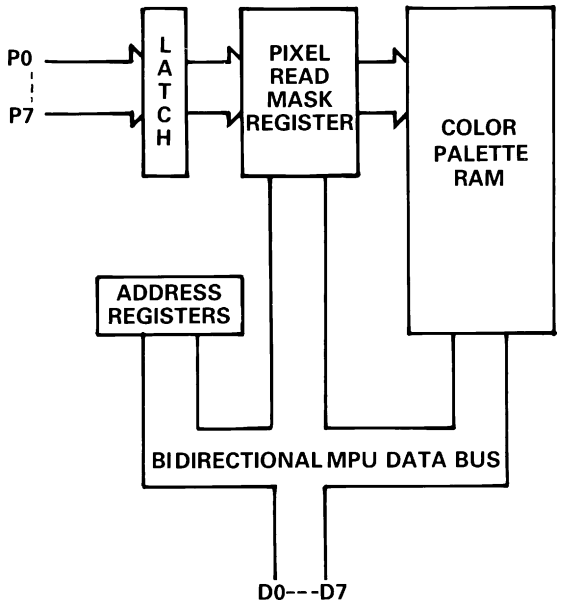



*Figure 3. Block Diagram Showing Pixel Read Mask Register*

**Analog Interface**

The ADV476 has three analog outputs, corresponding to the Red, Green and Blue video signals.

The Red, Green and Blue analog outputs of the ADV476 are high impedance current sources. Each one of these three RGB current outputs is capable of directly driving a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable. Figure 4a shows the required configuration for each of the three RGB outputs connected into a doubly-terminated 75 Ω load. This arrangement will develop RS-343A video output voltage levels across a 75 Ω monitor. A simple method of driving RS-170 video levels into a 75 Ω monitor is shown in Figure 4b. The output current levels of the DACs remain unchanged but the source termination resistance, $Z_S$ on each of the three DACs is increased from 75 Ω to 150 Ω.

More detailed information regarding load terminations for various output configurations, including RS-343A and RS-170, is available in an application note entitled "Video Formats & Required Load Terminations," available from Analog Devices.

Figure 5 shows the video waveforms associated with the three RGB outputs, driving the doubly terminated 75 Ω load of Figure 4a. The $\overline{\text{BLANK}}$ control input drives the analog outputs to the Black Level. $\overline{\text{BLANK}}$ is asserted prior to horizontal and vertical screen retrace. Table V details how the $\overline{\text{BLANK}}$ input modifies the output levels.

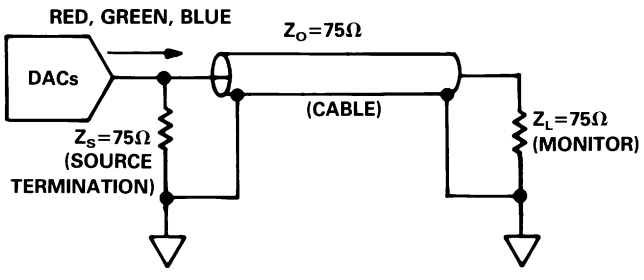



*Figure 4a. Recommended Analog Output Termination for RS-343A*

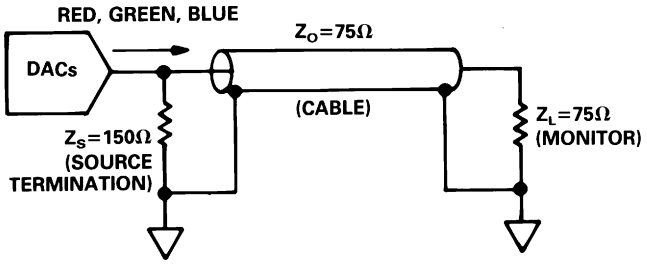
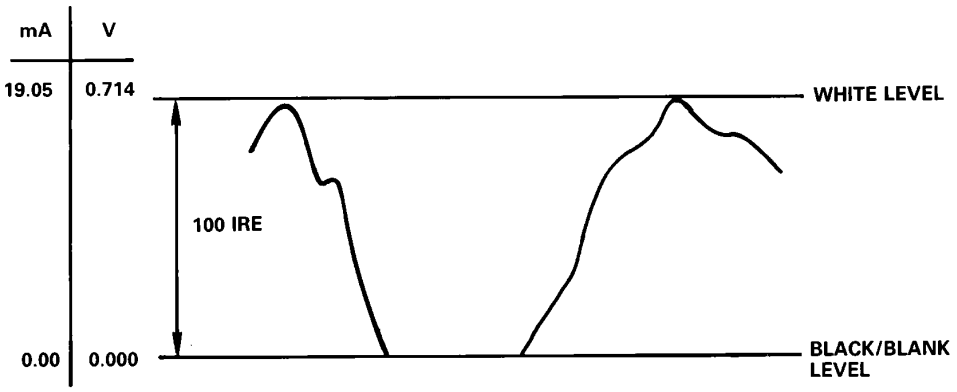



*Figure 4b. Recommended Analog Output Termination for RS-170*




NOTES
1. OUTPUTS CONNECTED TO A DOUBLY TERMINATED 75Ω LOAD.
2. $I_{REF}$=8.88mA.
3. RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

*Figure 5. RGB Video Output Waveform*

**Table V. Video Output Truth Table**

| Description | RED, GREEN, BLUE, (mA)[1] | $\overline{\text{BLANK}}$ | DAC Input Data |
|---|---|---|---|
| WHITE LEVEL | 19.05 | 1 | FFH |
| VIDEO | Video | 1 | DATA |
| BLACK LEVEL | 0 | 1 | 00H |
| BLANK LEVEL | 0 | 0 | xxH |

NOTE
[1]Typical with full Scale RED, GREEN, BLUE = 19.05 mA. $I_{REF}$ = 8.88 mA.

**Reference Input**

The ADV476 requires an active current reference to enable the DACs provide stable and accurate video output levels. The relationship between the output voltage and the required input reference current is given by:

$$I_{REF} = \frac{VO(FULL\ SCALE)}{2.15 \times R_L}$$

where $R_L$ = 37.5 Ω (for doubly terminated 75 Ω load)
= 75 Ω (for singly terminated 75 Ω load)

and $VO$ = 0.714 V (RS-343A video levels)
= 1.0 V (RS-170 video levels).

In a standard application which requires RS-343A video levels to be driven into a doubly terminated 75 Ω load ($R_L$ = 37.5 Ω), the necessary reference input current is:

$$I_{REF} = 8.88\ mA.$$

To drive the same levels into a singly terminated 75 Ω load ($R_L$ = 75 Ω), the reference current is:

$$I_{REF} = 4.44\ mA.$$

A suggested current reference design for the doubly terminated case, with RS-343A video levels and based on the LM334, a three-terminal adjustable current source, is shown in Figure 6.

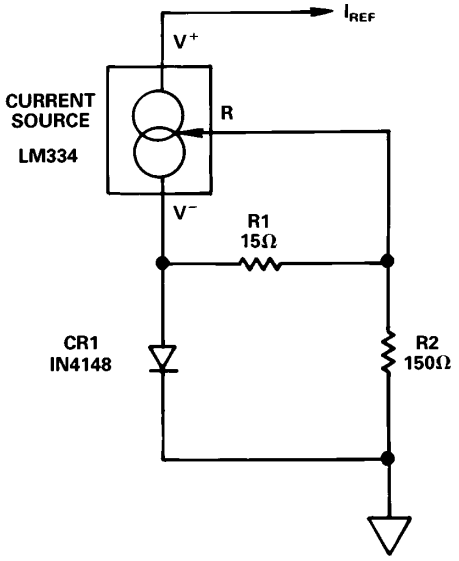



*Figure 6. Current Reference Design Using an LM334 Current Source*

## PC BOARD LAYOUT CONSIDERATIONS

The ADV476 is optimally designed for lowest noise performance, both radiated and conducted noise. For optimum system noise performance, it is imperative that great care be given to the PC board layout. The layout should be optimized for lowest noise on the ADV476 power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of $V_{CC}$ and GND pins should by minimized so as to minimize inductive ringing.

### Ground Planes

The ground plane should encompass all ADV476 ground pins, voltage reference circuitry, power supply bypass circuitry, the analog output traces and all the digital signal traces leading up to the ADV476.

### Power Planes

The PC board layout should have two distinct power planes, one for analog circuitry and one for digital circuitry. The analog power plane ($V_{CC}$) should encompass the ADV476 and all associated analog circuitry. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 7. This bead should be located within three inches of the ADV476.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV476 power pins, current reference circuitry and any output amplifiers.

The PCB power and ground planes should not overlay portions of the analog power plane. Keeping the PCB power and ground planes from overlaying the analog power plane will contribute to a reduction in plane-to-plane noise coupling.

### Supply Decoupling

Noise on the analog power plane can be further reduced by the use of multiple decoupling capacitors, see Figure 7.

Optimum performance is achieved by the use of 0.1 μF ceramic capacitors. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

It is important to note that while the ADV476 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise. A dc power supply filter (Murata BNX002) will provide EMI suppression between the switching power supply and the main PCB. Alternatively, consideration could be given to using a three terminal voltage regulator.

### Digital Signal Interconnect

The digital signal lines to the ADV476 should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the ADV476 should be avoided so as to minimize noise pickup.

Any active pull-up termination resistors for the digital inputs should be connected to the regular PCB power plane and not the analog power plane.

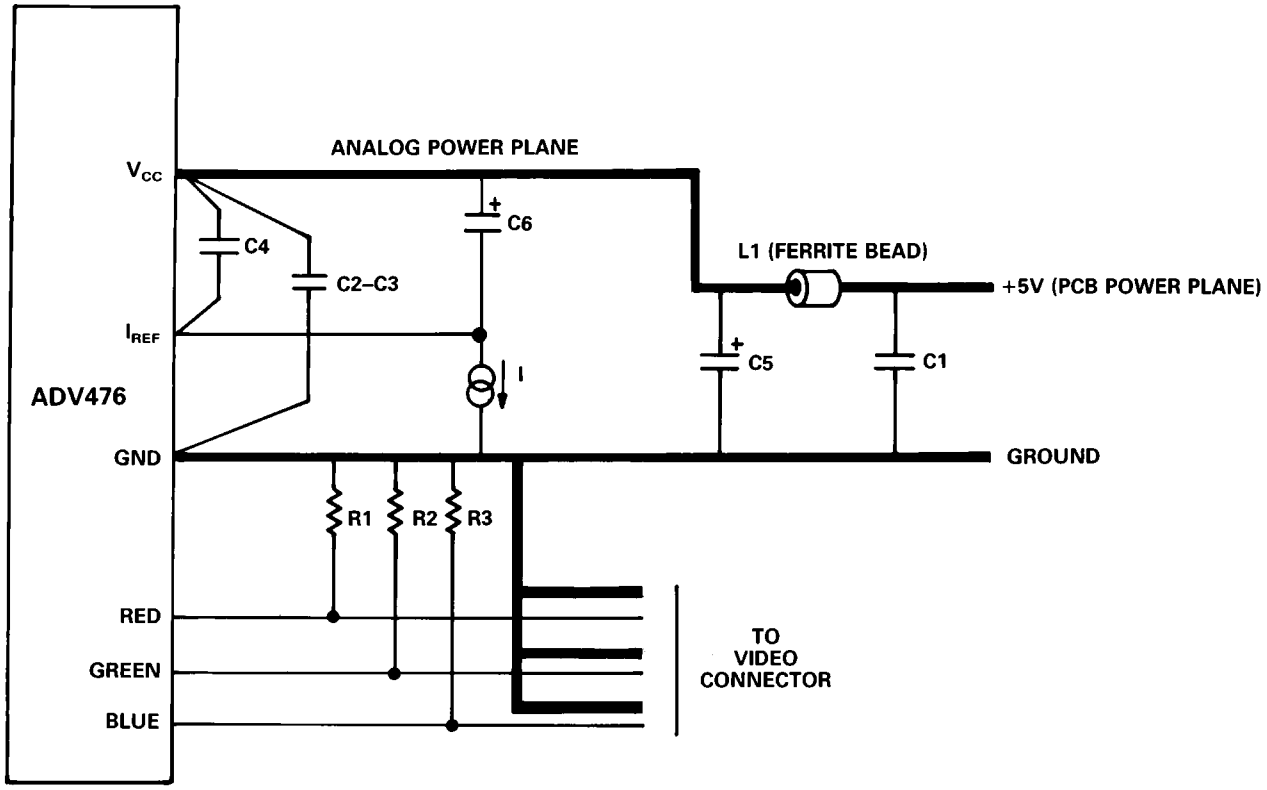
### Analog Signal Interconnect

The ADV476 should be located as close as possible to the output connectors thus minimizing noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, thereby maximizing the high frequency power supply rejection.

For optimum performance, the analog outputs should each have a source termination resistance to ground of 75 Ω. This termination resistance should be as close as possible to the ADV476 to minimize reflections.

Note: For additional information on PC Board-Layout see Application Note “Design and Layout of a Video Graphics System for Reduced EMI”, available from Analog Devices (Pub. No. E1309–15–10/89).




| COMPONENT | DESCRIPTION | VENDOR PART NUMBER |
|---|---|---|
| C1–C4 | 0.1μF CERAMIC CAPACITOR | ERIE RPE112Z5U104M50V |
| C5 | 10μF TANTALUM CAPACITOR | MALLORY CSR13G106KM |
| C6 | 47μF TANTALUM CAPACITOR | MALLORY CSR13F476KM |
| L1 | FERRITE BEAD | FAIR-RITE 2743001111 |
| R1, R2, R3 | 75Ω 1% METAL FILM RESISTOR | DALE CMF-55C |

*Figure 7. ADV476 Typical Connection Diagram and Component List*

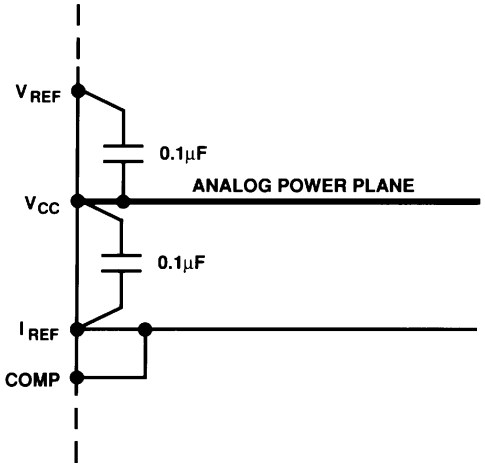
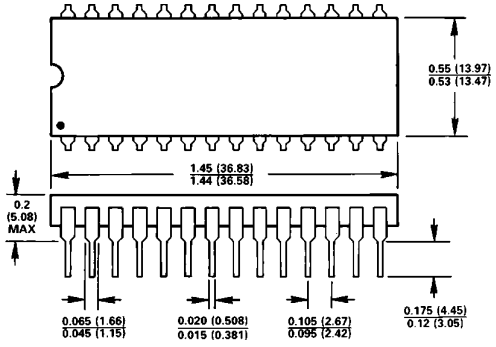



*Figure 8. Connection of $V_{REF}$ and COMP with the ADV476KP (44-Pin PLCC)*

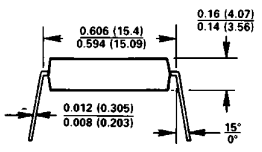
**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

**28-Pin Plastic DIP**
**(N-28)**




LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42



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