

Look-ahead carry generator

74F182

FEATURES

- Provides carry look-ahead across a group of four ALUs
- Multi-level look-ahead for high speed arithmetic operation over long word lengths

DESCRIPTION

The 74F182 is a high speed carry look-ahead generator. It accepts up to four pairs of active-Low Carry Propagate ($\overline{P}0, \overline{P}1, \overline{P}2, \overline{P}3$) and Carry Generate ($\overline{G}0, \overline{G}1, \overline{G}2, \overline{G}3$) signals and an active-High Carry input (C_n) and provides anticipated active-High carries ($C_{n+x}, C_{n+y}, C_{n+z}$) across four groups of binary adders. The 74F182 also has active-Low Carry Propagate (\overline{P}) Carry Generate (\overline{G}) outputs which may be used for further levels of look-ahead.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0 C_n$$

$$C_{n+y} = G_1 + P_1 G_0 + P_1 P_0 C_n$$

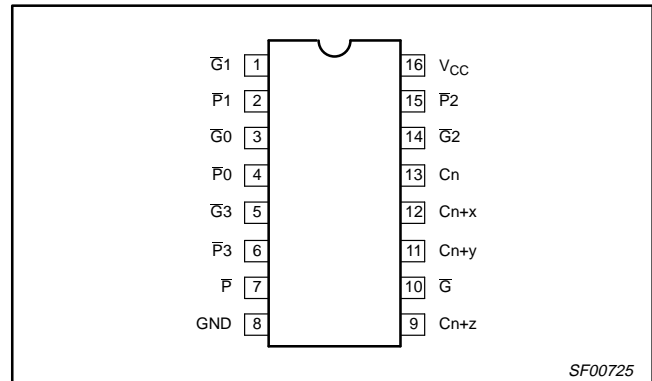
$$C_{n+z} = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n$$

$$\overline{G} = \overline{G}_3 + P_3 \overline{G}_2 + P_3 P_2 \overline{G}_1 + P_3 P_2 P_1 \overline{G}_0$$

$$\overline{P} = P_3 P_2 P_1 P_0$$

The 74F182 can also be used with binary ALUs in an active-Low or active-High input operand mode. The connections to and from the ALU to the carry look-ahead generator are identical in both cases.

PIN CONFIGURATION



SF00725

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|--------|---------------------------|--------------------------------|
| 74F182 | 5.0ns | 21mA |

ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|--------------------|---|
| | COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^\circ C$ to $+70^\circ C$ |
| 16-pin plastic DIP | N74F182N |
| 16-pin plastic SO | N74F182D |

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74FAST (U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|--------------------------------|-------------------------------------|------------------------|---------------------|
| C_n | Carry input | 2.5/2.0 | 50 μ A/1.2mA |
| $\overline{G}0, \overline{G}2$ | Carry generate inputs (active-Low) | 2.5/14.0 | 50 μ A/8.4mA |
| $\overline{G}1$ | Carry generate input (active-Low) | 2.5/16.0 | 50 μ A/9.6mA |
| $\overline{G}3$ | Carry generate input (active-Low) | 2.5/8.0 | 50 μ A/4.8mA |
| $\overline{P}0, \overline{P}1$ | Carry propagate inputs (active-Low) | 2.5/8.0 | 50 μ A/4.8mA |
| $\overline{P}2$ | Carry propagate input (active-Low) | 2.5/6.0 | 50 μ A/3.6mA |
| $\overline{P}3$ | Carry propagate input (active-Low) | 2.5/4.0 | 50 μ A/2.4mA |
| $C_{n+x} - C_{n+z}$ | Carry outputs | 50/33 | 1.0mA/20mA |
| \overline{G} | Carry generate output (active-Low) | 50/33 | 1.0mA/20mA |
| \overline{P} | Carry propagate output (active-Low) | 50/33 | 1.0mA/20mA |

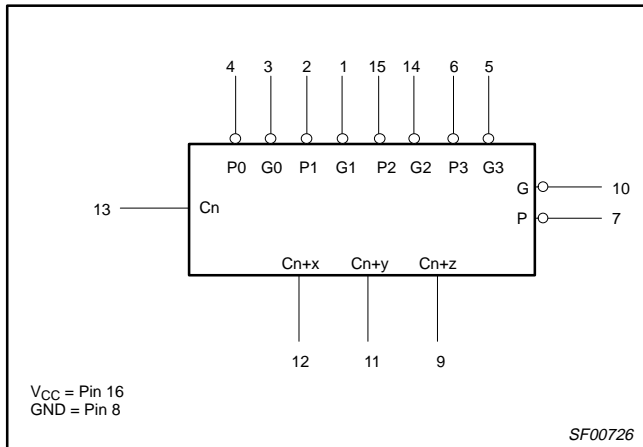
NOTE:

One (1.0) FAST unit load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

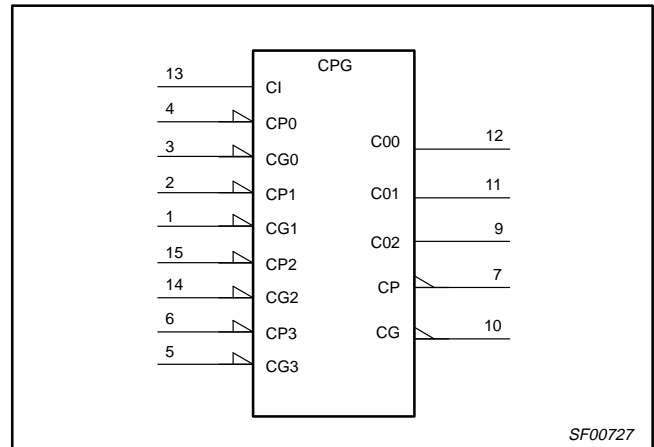
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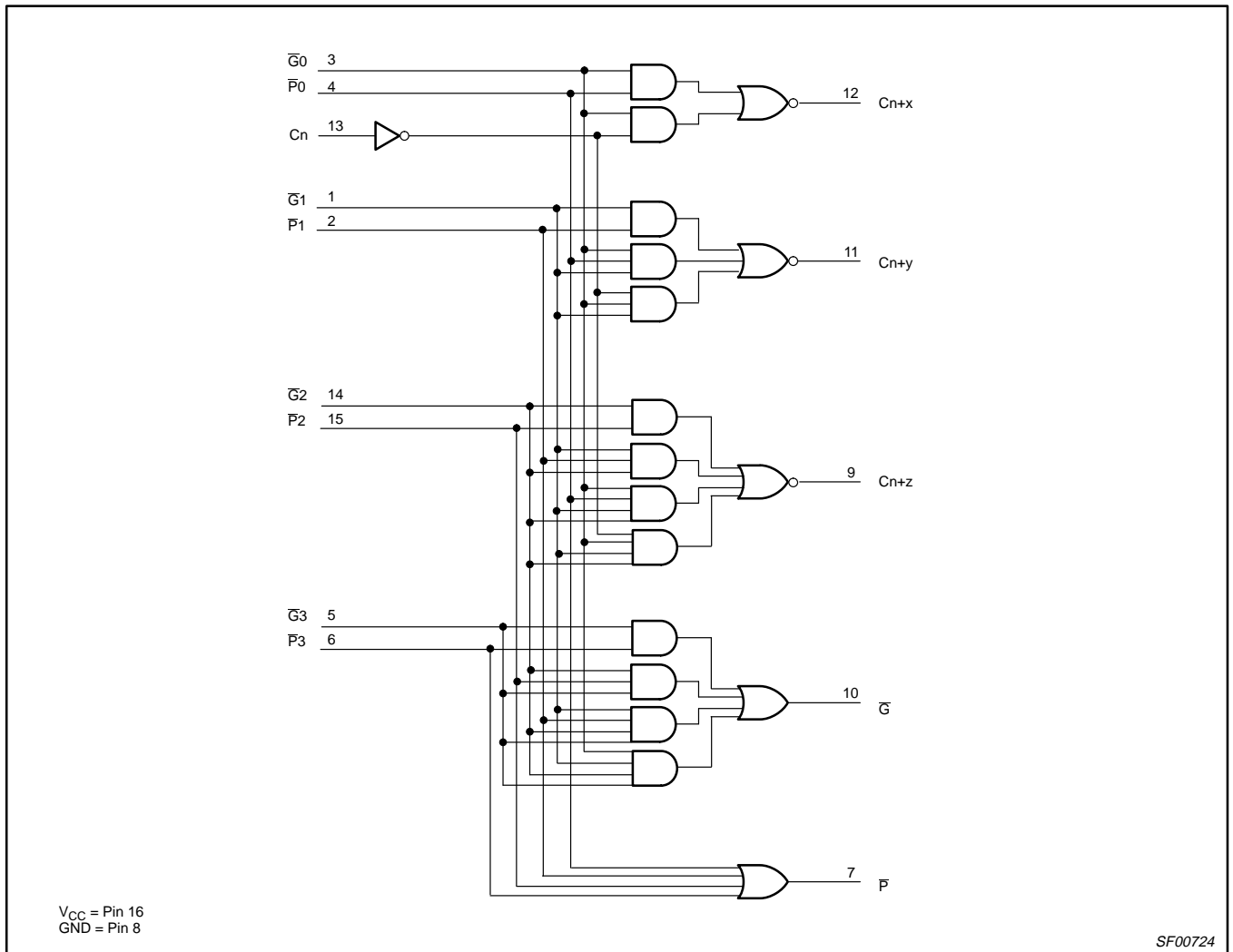
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



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FUNCTION TABLE

| INPUTS | | | | | | | | | OUTPUTS | | | | |
|--------|----|----|----|----|----|----|----|----|---------|------|------|---|---|
| Cn | G0 | P0 | G1 | P1 | G2 | P2 | G3 | P3 | Cn+x | Cn+y | Cn+z | G | P |
| X | H | H | | | | | | | L | | | | |
| L | H | X | | | | | | | L | | | | |
| X | L | X | | | | | | | H | | | | |
| H | X | L | | | | | | | H | | | | |
| X | X | X | H | H | | | | | | L | | | |
| X | H | H | H | X | | | | | | L | | | |
| L | H | X | H | X | | | | | | L | | | |
| X | X | X | L | X | | | | | | H | | | |
| X | L | X | X | L | | | | | | H | | | |
| H | X | L | X | L | | | | | | H | | | |
| X | X | X | X | X | H | H | | | | | L | | |
| X | X | X | H | H | H | X | | | | | L | | |
| X | H | H | H | X | H | X | | | | | L | | |
| L | H | X | H | X | H | X | | | | | L | | |
| X | X | X | X | X | L | X | | | | | H | | |
| X | X | X | L | X | X | L | | | | | H | | |
| X | L | X | X | L | X | L | | | | | H | | |
| H | X | L | X | L | X | L | | | | | H | | |
| | X | | X | X | X | X | H | H | | | | H | |
| | X | | X | X | H | H | H | X | | | | H | |
| | X | | H | H | H | X | H | X | | | | H | |
| | H | | H | X | H | X | H | X | | | | H | |
| | X | | X | X | X | X | L | X | | | | L | |
| | X | | X | X | L | X | X | L | | | | L | |
| | X | | L | X | X | L | X | L | | | | L | |
| | L | | X | L | X | L | X | L | | | | L | |
| | | H | | X | | X | | X | | | | | H |
| | | X | | H | | X | | X | | | | | H |
| | | X | | X | | H | | X | | | | | H |
| | | X | | X | | X | | H | | | | | H |
| | | L | | L | | L | | L | | | | | L |

NOTES:

- H = High voltage level
- L = Low voltage level
- X = Don't care

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APPLICATION

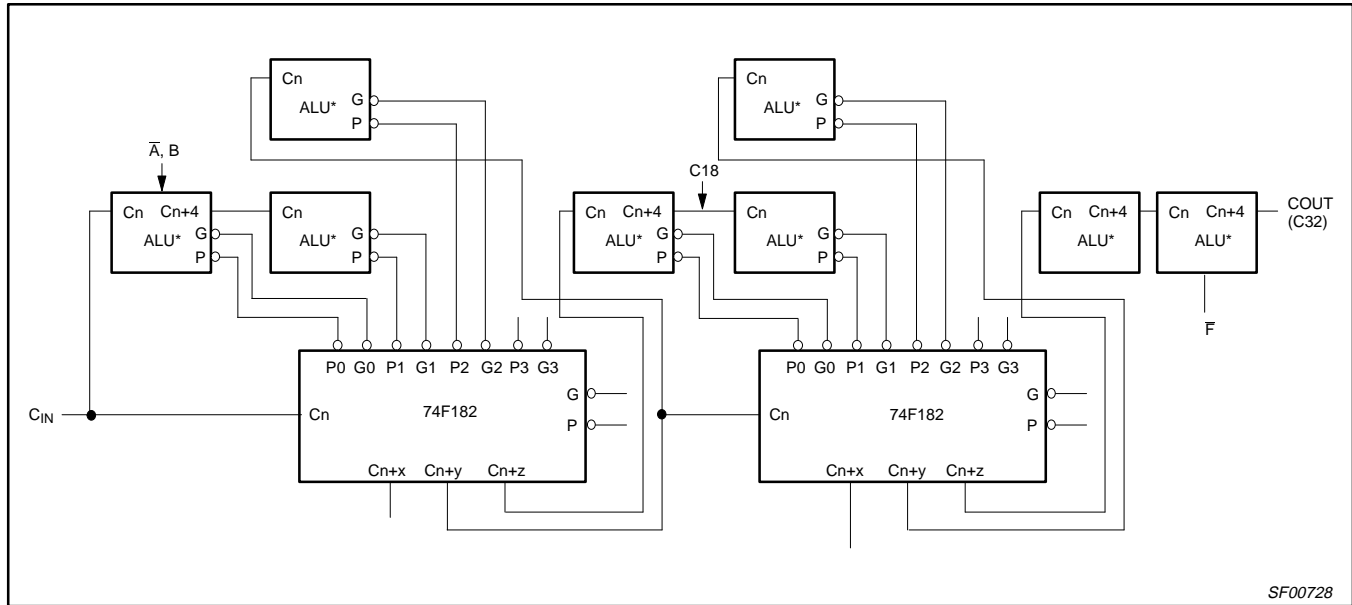


Figure 1. 32-Bit ALU with Ripple Carry Between 16-Bit Look-Ahead ALUs (*ALUs may be either 74F181 or 74F381)

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

| SYMBOL | PARAMETER | RATING | UNIT |
|------------------|--|-------------------------|------|
| V _{CC} | Supply voltage | -0.5 to +7.0 | V |
| V _{IN} | Input voltage | -0.5 to +7.0 | V |
| I _{IN} | Input current | -30 to +5 | mA |
| V _{OUT} | Voltage applied to output in High output state | -0.5 to V _{CC} | V |
| I _{OUT} | Current applied to output in Low output state | 40 | mA |
| T _{amb} | Operating free-air temperature range | 0 to +70 | °C |
| T _{stg} | Storage temperature range | -65 to +150 | °C |

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|------------------|--------------------------------------|--------|-----|-----|------|
| | | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | High-level input voltage | 2.0 | | | V |
| V _{IL} | Low-level input voltage | | | 0.8 | V |
| I _{IK} | Input clamp current | | | -18 | mA |
| I _{OH} | High-level output current | | | -1 | mA |
| I _{OL} | Low-level output current | | | 20 | mA |
| T _{amb} | Operating free-air temperature range | 0 | | 70 | °C |

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | TEST CONDITIONS ¹ | | LIMITS | | | UNIT | |
|-----------------|---|--|---|---------------------|------------------|------|------|----|
| | | | | MIN | TYP ² | MAX | | |
| V _{OH} | High-level output voltage | V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN | I _{OH} = MAX | ±10%V _{CC} | 2.5 | | V | |
| | | | | ±5%V _{CC} | 2.7 | 3.4 | V | |
| V _{OL} | Low-level output voltage | V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN | I _{OL} = MAX | ±10%V _{CC} | | 0.30 | 0.50 | V |
| | | | | ±5%V _{CC} | | 0.30 | 0.50 | V |
| V _{IK} | Input clamp voltage | V _{CC} = MIN, I _I = I _{IK} | | | -0.73 | -1.2 | V | |
| I _I | Input current at maximum input voltage | V _{CC} = MAX, V _I = 7.0V | | | | 250 | μA | |
| I _{IH} | High-level input current | V _{CC} = MAX, V _I = 2.7V | | | | 250 | μA | |
| I _{IL} | Low-level input current | V _{CC} = MAX, V _I = 0.5V | C _n | | | | -1.2 | mA |
| | | | $\overline{G}0, \overline{G}2$ | | | | -8.4 | mA |
| | | | $\overline{G}1$ | | | | -9.6 | mA |
| | | | $\overline{G}3, \overline{P}0, \overline{P}1$ | | | | -4.8 | mA |
| | | | $\overline{P}2$ | | | | -3.6 | mA |
| | | | $\overline{P}3$ | | | | -2.4 | mA |
| I _{OS} | Short-circuit output current ³ | V _{CC} = MAX | | | -60 | -150 | mA | |
| I _{CC} | Supply current (total) | V _{CC} = MAX | | | 18 | 28 | mA | |
| | | I _{CCH} | | | 24 | 36 | mA | |
| | | I _{CCL} | | | | | | |

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

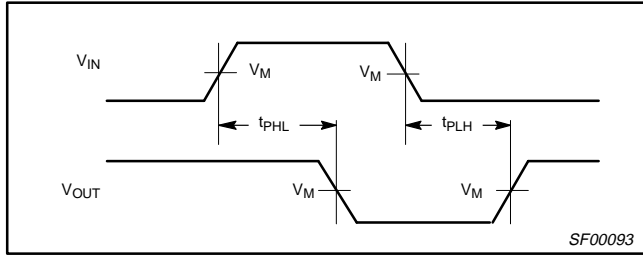
| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | | | | UNIT |
|--------------------------------------|--|----------------|---|------------|-------------|--|-------------|----|------|
| | | | V _{CC} = +5.0V T _{amb} = +25°C C _L = 50pF R _L = 500Ω | | | V _{CC} = +5.0V ± 10% T _{amb} = 0°C to +70°C C _L = 50pF R _L = 500Ω | | | |
| | | | MIN | TYP | MAX | MIN | MAX | | |
| t _{PLH} t _{PHL} | Propagation delay C _n to C _{n+x} , C _{n+y} , C _{n+z} | Waveform 2 | 2.5 2.5 | 5.0 5.0 | 8.0 7.5 | 2.5 2.5 | 8.5 8.5 | ns | |
| t _{PLH} t _{PHL} | Propagation delay $\overline{P}0, \overline{P}1, \text{ or } \overline{P}2$ to C _{n+x} , C _{n+y} , C _{n+z} | Waveform 1 | 2.0 1.5 | 5.0 3.5 | 7.0 5.0 | 1.5 1.5 | 8.0 6.0 | ns | |
| t _{PLH} t _{PHL} | Propagation delay $\overline{G}0, \overline{G}1, \text{ or } \overline{G}2$ to C _{n+x} , C _{n+y} , C _{n+z} | Waveform 1 | 1.5 1.5 | 4.0 3.0 | 7.5 5.0 | 1.5 1.5 | 8.5 5.5 | ns | |
| t _{PLH} t _{PHL} | Propagation delay $\overline{P}1, \overline{P}2, \text{ or } \overline{P}3$ to \overline{G} | Waveform 2 | 2.0 3.0 | 7.0 5.0 | 10.0 7.0 | 1.5 2.5 | 11.0 8.0 | ns | |
| t _{PLH} t _{PHL} | Propagation delay $\overline{C}n$ to \overline{G} | Waveform 2 | 1.5 3.0 | 5.0 5.0 | 7.0 7.0 | 1.5 2.5 | 7.5 8.0 | ns | |
| t _{PLH} t _{PHL} | Propagation delay $\overline{P}n$ to \overline{P} | Waveform 2 | 1.5 2.5 | 3.5 4.0 | 6.0 6.0 | 1.5 2.5 | 7.5 6.5 | ns | |

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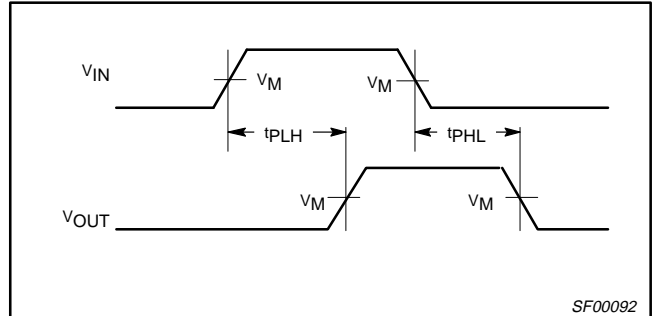
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AC WAVEFORMS

For all waveforms, $V_M = 1.5V$

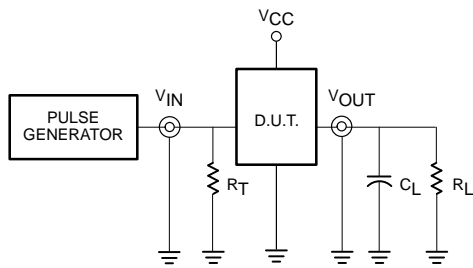


Waveform 1. Propagation Delay for Inverting Outputs

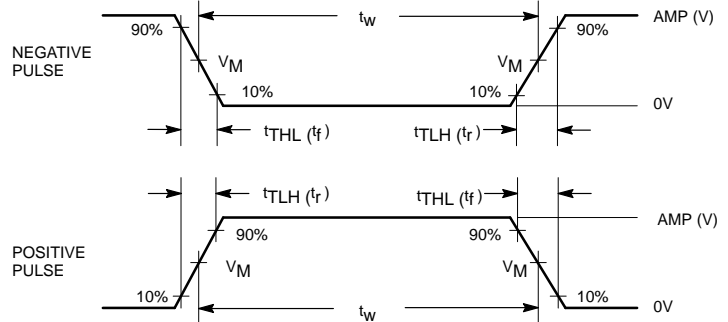


Waveform 2. Propagation Delay for Non-Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS:

- R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

| family | INPUT PULSE REQUIREMENTS | | | | | |
|--------|--------------------------|-------|-----------|-------|-----------|-----------|
| | amplitude | V_M | rep. rate | t_w | t_{TLH} | t_{THL} |
| 74F | 3.0V | 1.5V | 1MHz | 500ns | 2.5ns | 2.5ns |

SF00006